

A Time-Resolved, Low-Noise Single-Photon Image Sensor Fabricated in Deep-Submicron CMOS Technology

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Abstract—We report on the design and characterization of a novel time-resolved image sensor fabricated in a 130 nm CMOS process. Each pixel within the 32×32 pixel array contains a low-noise single-photon detector and a high-precision time-to-digital converter (TDC). The 10-bit TDC exhibits a timing resolution of 119 ps with a timing uniformity across the entire array of less than 2 LSBs. The differential non-linearity (DNL) and integral non-linearity (INL) were measured at ± 0.4 and ± 1.2 LSBs, respectively. The pixel array was fabricated with a pitch of $50 \mu\text{m}$ in both directions and with a total TDC area of less than $2000 \mu\text{m}^2$. The target application for this sensor is time-resolved imaging, in particular fluorescence lifetime imaging microscopy and 3D imaging. The characterization shows the suitability of the proposed sensor technology for these applications.

Index Terms—Single-photon imaging, single-photon avalanche diode, SPAD, time-to-digital converter, TDC, time-resolved imaging, time-of-flight, fluorescence lifetime imaging microscopy, FLIM, fluorescence correlation spectroscopy, FCS.

I. INTRODUCTION

TIME-RESOLVED imaging has been a rapidly growing field of investigation in recent years as it offers several advantages over traditional intensity imaging in the life sciences, for example, where it has enabled the emergence of fluorescence lifetime imaging microscopy (FLIM), a quantitative imaging method to locally probe the chemical environment of a fluorophore in living cells. So far, most time-correlated single-photon counting (TCSPC) setups were based on a single detector, often a silicon photomultiplier (SiPM) or a single-photon avalanche diode (SPAD) [1], an external chronometer, often a

time-to-digital converter (TDC) [2]–[4], and an optical scanner to reconstruct an image. The integration of SPADs in CMOS technology [5] has significantly improved the level of miniaturization of SPADs and thus paved the way for large SPAD arrays [6]. Early implementations of SPAD arrays however did not integrate TDCs on chip and thus only one pixel was active at a time [6], [7]. Later, larger SPAD arrays (128×128) were integrated with up to 32 parallel TDCs allowing an entire row of pixels to be active simultaneously [8]. However, in order to acquire fast images over the entire array it is necessary to integrate many more TDCs on chip, possibly one per detector, so as to enable independent and simultaneous acquisition and time discrimination at the pixel basis. To achieve this, very compact TDCs must be designed. However, due to the complexity of these devices, only a deep-submicron implementation may be a viable alternative.

In this paper we report on the design and characterization of an array of 1024 time-resolved pixels implemented in a 130 nm imaging CMOS process [9]. Each TDC was coupled to a low noise SPAD based on [10] and [11]. To the best of our knowledge, to date, this is one of the largest arrays of fully integrated time-resolved pixels ever built and the TDC array with the highest individual conversion throughput. The array consists of 1024 pixels, independently and simultaneously operating at a global rate of 500 MS/s. The current readout speed is limited by the external hardware. While the chip allows for a frame rate of 1 M frame-per-second (fps), it is currently operated at 500 kfps. Each TDC/SPAD ensemble measures only $50 \times 50 \mu\text{m}^2$. It is thus one of the smallest ever demonstrated with deep sub-nanosecond resolution.

II. DETECTION AND TIME-TO-DIGITAL CONVERSION

A. State-of-the-Art in Integrated Time-to-Digital Conversion

In many applications, such as optical rangefinding, 3-D imaging, time-of-flight positron emission tomography (PET) or, as targeted here, FLIM, it is critical to measure photon time-of-arrival. In our solution, the SPAD ensemble is used to convert a photon arrival onto an electrical pulse. TDCs are used to measure the time elapsed between that pulse (conventionally known as “START”) and a reference signal (“STOP”) that is subsequently converted onto a code. In the case of FLIM, the reference signal is given by the laser synchronization signal.

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Extensive literature exists on TDC architecture [2]–[15]. The vast majority of published devices function as stand-alone custom integrated circuits. Thus, in such devices, the requirements on area and power are relaxed. In this work, the TDC must fit in a pixel with lateral dimensions of $50 \times 50 \mu\text{m}^2$; in the same space the SPAD ($15 \times 15 \mu\text{m}^2$), a 10-bit memory block, and readout and glue electronics must also be fitted. At the same time, the fabrication of an array of pixels requires that a strict in-pixel power budget be kept to minimize IR drops and di/dt effects across the array. Supply voltage ripple could result in an increased non-homogeneity in performance, as well as systematic errors and fix pattern noise. However, FLIM requires neither extremely high time resolution nor extended range of operation but high linearity and conversion rate. A TDC with a resolution of 100 ps, a range of less than 100 ns, a conversion rate of 500 kS/s pixel, and a differential non-linearity better than ± 0.4 LSB is thus sufficient for almost all FLIM applications.

In principle, an extremely simple implementation of a TDC could consist of a high-frequency clock and a counter incremented at each clock edge. In such a case, the resolution would be given by the clock period and the accuracy by the stability of the clock and of the clock stopping method. A simple PLL can guarantee a stable clock at high frequency and it is available as a standard cell in many CMOS processes. Unfortunately, in this simple implementation a clock frequency $f_{\text{clock}} = 1/\Delta t$ is needed for a resolution Δt . For example $\Delta t = 100$ ps implies $f_{\text{clock}} = 10$ GHz. While this frequency has been generated in some recent CMOS radio-frequency circuits, its use and distribution across a large array of pixels poses several problems at various levels, particularly noise, crosstalk, and power dissipation.

An alternative is the use of a pulse-length preserving Vernier delay line [3], [16]. Logic buffers can be used as the elementary delay unit and the resolution of the delay line is given by the buffer's gate delay. In most cases, the delay line is used in conjunction with a DLL to stabilize the delay line against process, voltage, and temperature variations (PVT). On the start signal a pulse is sent through the delay line and it propagates until the delay line is "frozen" upon receiving the stop signal. The propagation can be stopped for example by using a pass-gate between delay elements or by using tri-state buffers. Unfortunately, metastability issues may arise in such delay lines in the case the pulse propagation is stopped during the switching of a buffer. To ensure reliable measurements in the worst-case scenario, the individual buffer delays must often be increased from their nominal minimum value, therefore reducing the intrinsic timing resolution.

To reduce the area of the TDC, thus allowing each pixel to operate independently and simultaneously, a significant downsizing of the TDC area must be achieved. In terms of electronic design, a simple way to reduce the area is to move from a sub-micron to a deep-submicron CMOS process. However, in terms of detector design, several new challenges appear, as detailed in [10]. A good compromise between TDC and SPAD design was found by using a 130 nm imaging CMOS process provided by ST Microelectronics. Additionally, a drastic reduction of complexity cannot be avoided – limiting the TDC to its most essen-

tial components while the performance must be maintained at an acceptable level.

B. TDC Requirements and Solutions

To assess the requirements for the TDC let us first consider the total timing jitter and their origins for a single pixel. Assuming statistically independent noise contributions, $\sigma_{\text{TOT}} = \sqrt{\sigma_q^2 + \sigma_{\text{START}}^2 + \sigma_{\text{STOP}}^2 + \sigma_{\text{TDC}}^2}$, with σ_q the quantization error, σ_{START} and σ_{STOP} the timing jitter on the start and stop signals respectively, and σ_{TOT} the total jitter of the different elements within the TDC. It is known from [17] that the timing jitter of the start signal given by the SPAD is of the order of 100 ps. As a consequence, since the other timing uncertainties sum up as root-mean-square, any other lower jitter contribution will be dominated by it. Most FLIM applications require a time resolution in the order of 100–200 ps, as the vast majority of fluorophores have a lifetime in the low nanosecond range. Thus the specifications on time resolution and jitter for an in-pixel TDC can be set to less than 150 ps.

As mentioned previously, delay line based TDC implementations allow for reliable TDC implementations with a heavily technology-limited resolution given by the delay of a single element. More complex implementations, yielding sub-gate delay resolution, do not match the area constraints and are thus disregarded. However, to achieve a reasonable time range, an extremely long delay line is required. As an example, 500 delay units are required for a range of 50 ns and 100 ps of resolution. The obvious solution is to implement a ring oscillator instead of a single line [18]; the drawback of this solution is an increased mismatch between the delay elements as all the buffers cannot be placed in the same direction and an inherently higher jitter.

Let us look at the jitter more in detail. For both a delay line and a ring oscillator implementation, the TDC time jitter σ_{TDC} is continuously accumulated during the acquisition process. Assuming an identical, independent distribution (i.i.d.), the jitter in a delay line is given by

$$\sigma_{\text{TDC}} = \sqrt{\sum_{i=1}^n \sigma_{\text{AV}_j}^2} = \sqrt{n} \sigma_{\text{AV}_j}$$

where n is the number of delay units switching for a particular measurement and σ_{AV_j} is the average time jitter of a single buffer. A similar argument can be made for the case of ring oscillators, whereas n is given by $n = C + n_{\text{res}}$, with C being the number of cycles occurring from start to stop and n_{res} the residual number of delay elements in the ring. Note that in a ring oscillator, the assumption of statistical independence between delay elements is no longer accurate after the first cycle is complete.

It is important to note that the time jitter is thus heavily dependent on the interval length to be measured; long time intervals measurements will yield a significantly higher time uncertainty. To keep σ_{AV_j} within acceptable bounds it is common practice to embed the delay line into a DLL providing a reference voltage, which controls the current flow in the delay elements, and thus regulates the unitary delay across process, voltage and tempera-

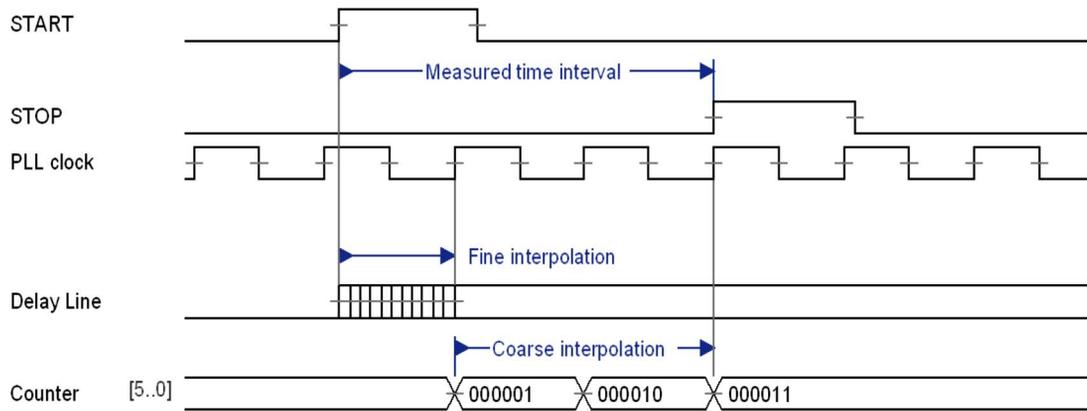


Fig. 1. Timing diagram of the in-pixel TDC. The coarse time measurement is achieved by incrementing a 6-bit counter on each rising clock edge. The fine interpolation is measured by starting the propagation of the start pulse in a 16-element delay chain and stopping the propagation on the first subsequent rising clock edge.

ture variations. In this design, embedding an in-pixel DLL was not an option, thus we opted for a feed-forward solution where the delay of the in-pixel delay line is globally controlled to cope for temperature and voltage supply variations. In our measurements, performed in photon-starved mode, we found that intra-die process variations were too insignificant to require a more complex calibration system. Though, in situations of high illumination, it is possible that a pixel with a high photon rate will draw significantly larger current and thus it may locally heat up, possibly reducing the supply voltage, thus affecting it and the neighboring pixels.

C. In-Pixel TDC Architecture

The high-frequency clock distribution with in-pixel counter scheme achieves a very good timing jitter and uniformity since the clock can be generated very precisely with the use of a PLL while the clock distribution can be addressed by proper design of a clock tree and careful analysis of the clock path. The main drawback of this technique is the high clock frequency required and the excessive power consumption for clock distribution, scaling quadratically with the supply voltage and linearly with the clock frequency and the load capacitance.

Because of the above considerations, we propose a two-level interpolator with a coarse resolution given by a low-frequency clock and a short delay line capable of resolving time intervals shorter than the clock period. This approach limits the power consumption by significantly reducing the clock frequency and, at the same time, the accumulated jitter. PVT variations encountered by long-range delay lines are kept within reasonable bounds by limiting the range to one clock cycle. The timing diagram of the proposed TDC is shown in Fig. 1. The clock required for the coarse interpolator (a 6-bit counter) is generated on-chip by means of an on-chip PLL through a balanced clock distribution network. The low-frequency input clock to the PLL is given by an external clock to allow for synchronization with a laser for FLIM experiments. The laser synchronization clock is also used as STOP signal, thus the STOP signal and the clock generated by the PLL have a constant delay, and a second fine interpolation is not required at the end of the measured time interval.

To increase the coarse resolution, the clock signal (CLK) is doubled in-pixel to 560 MHz. Local frequency doubling is implemented to reduce the power dissipation, crosstalk and other undesired effects caused by the clock distribution. Fig. 2 shows the coarse interpolator and in-pixel frequency doubler. The dynamic power dissipation is estimated as $P_{\text{dyn}} \cong (C_{\text{clock_distrib}} + 2 \cdot 32^2 C_{\text{in_pixel}}) \cdot 280 \times 10^6 \cdot (1.2\text{V})^2$ [W] where $C_{\text{clock_distrib}}$ and $C_{\text{in_pixel}}$ are the capacitances driven by the clock distribution network and the voltage supply is assumed to be 1.2 V. With proper selection of these values, it is thus possible to find a good compromise in terms of power, while the use of in-pixel doublers ensures that heat sources could be distributed more uniformly across the array thus improving overall reliability. The 6-bit ripple counter is enabled by the START signal and disabled by the STOP signal, thus counting all clock pulses in the corresponding time interval. The coarse resolution is given by the clock period, 1.79 ns in the standard regime of operation. The circuit can also be used as a time-uncorrelated photon counter by acting on the multiplexer via the MODE signal; in this case, the output of the SPAD is directly connected to the clock of the counter.

The fine interpolator consists of a 16-element delay line, shown in Fig. 3. While a delay line consisting of inverters would guarantee the fastest propagation speed and resolution, the mismatch resulting from different rise and fall times would significantly degrade DNL. Therefore, a buffer-based delay line was implemented. The buffers consist, for area occupation reasons, of only five transistors and have a differential input pair to guarantee a first-order rejection of power supply and substrate noise.

The gate voltage VBIAS of the current-starving transistor allows adjusting the delay of the buffer cells. In most cases VBIAS is used to correct for PVT variations, it can however be used to increase the delay as well, in order to extend the range of the TDC. The width of the transistors is significantly larger than the minimum width of $0.15 \mu\text{m}$, not only to increase the drive strength, but also to provide a good matching of the differential input pair and good $1/f$ noise performance. Even though large transistor sizes are used, the implementation in an advanced CMOS process is still beneficial in terms of matching, as the mismatch for a given transistor size is improved [19]. Signifi-

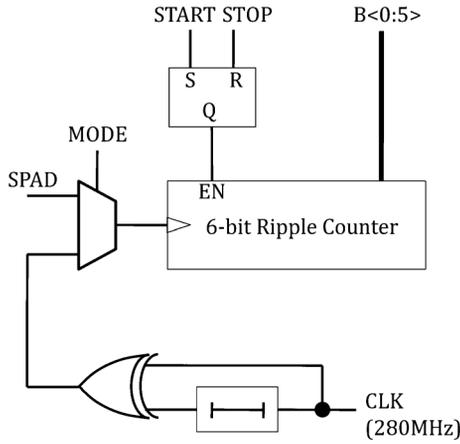


Fig. 2. Schematic of the in-pixel coarse interpolator. The clock from the PLL (CLK) is frequency-doubled within the pixel and fed into a multiplexer. The clock is directed into a 6-bit ripple counter based on scan flip-flops. The enable signal EN is high during the START-STOP time interval to be measured. Signal MODE forces the output of the SPAD to increment the counter, thereby achieving time-uncorrelated photon counting.

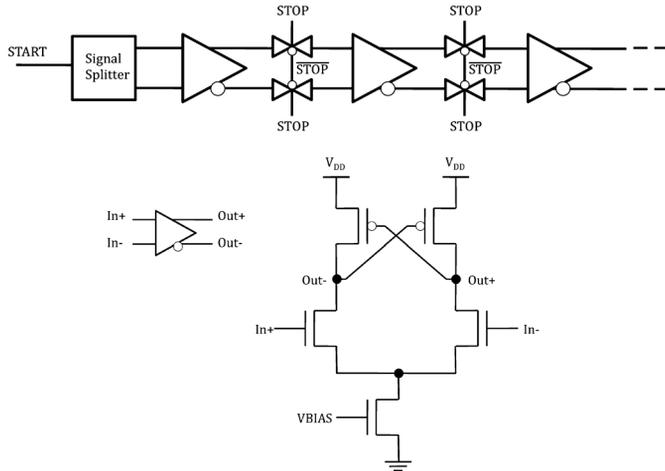


Fig. 3. Schematic of the fine interpolator delay line (16 elements) and of a single delay unit.

cant attention was placed on the layout of the delay chain. For example, all clock signals were placed at a significant distance, the 16th delay element acts as dummy cell to guarantee that all 15 active elements have the same load and the transistors were all placed in the same direction. In addition, the power supply grid was carefully designed in order to minimize IR drops, while di/dt effects were minimized by the use of a pixel-level decoupling capacitance.

D. Detector Ensemble

The deep-submicron SPAD (from [11]) is integrated alongside the required electronics for avalanche quenching, SPAD recharge, SPAD activation/deactivation as well as readout. A SPAD is a pn junction biased above its breakdown voltage, V_{BD} , by a voltage known as excess bias voltage V_E . Fig. 4 shows the SPAD ensemble; in idle mode, the voltage at the cathode of the diode stands at V_E , since the current across transistor P2 is negligible and VQUENCH is set so as the transistor is operating in sub-threshold regime. Upon photon de-

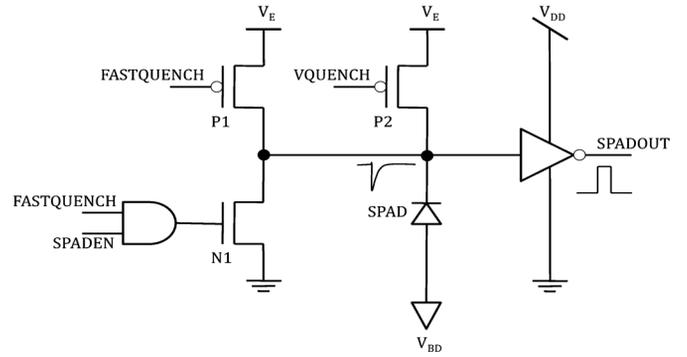


Fig. 4. Simplified schematic of the SPAD ensemble. The SPAD is a pn junction biased above breakdown through voltages V_E and V_{BD} . Upon a photon detection or a thermal event, an avalanche current is triggered and builds up until a non-linear ballast resistance (implemented by P2) quenches it. Transistors P1 and N1 are used to deactivate and reactivate the device for gated operation, while the inverter acts as a pulse-shaping buffer.

tection or a thermal event, an avalanche may be triggered; the avalanche current flows through transistor P2, that quickly enters linear mode of operation, thus decreasing the voltage seen at the cathode. With the build-up of the avalanche current, the voltage across the SPAD decreases to a value close to the breakdown voltage, at which point the avalanche multiplication is no longer sustained. Hence the avalanche current decreases exponentially and eventually drops to near-zero. At this point, the SPAD parasitic capacitance is recharged through the same transistor P2. In essence, P2 acts as a non-linear resistance for both the quenching and recharge of the SPAD and its value can be controlled through VQUENCH. The analog signal at the cathode is converted into a digital pulse by a simple inverter, which is subsequently processed by the in-pixel electronics. The inverter acts as a pulse shaper and impedance adapter. To allow for time-gated operation, the detector can be disabled through N1 by bringing the potential of the cathode below breakdown, thus bringing the optical gain from infinity (Geiger mode of operation) to a value near one (conventional reverse-biased photodiode). To reactivate the detector, the cathode is charged rapidly through P1, thus bringing the optical gain back to virtual infinity. To ensure that P1 and N1 are never active simultaneously, thus causing a direct current path from V_E to ground, the signals FASTQUENCH and SPADEN are used to control the gate of N1. Note that FASTQUENCH is an active low signal.

E. Pixel Architecture

A simplified block diagram of the full pixel is shown in Fig. 5, the main components are the detector ensemble, the TDC (consisting of the delay line, thermometer coder and the counter), the 10-bit memory, the readout buffers, the frequency doubler, and a flip-flop responsible to stop the fine interpolator (signal “sync” in the figure) and to start the coarse interpolator. When the fine interpolator is stopped, the propagation of the START signal is frozen. The time interval is thermometer-coded and it is converted to binary on-pixel to save output lines. The signal STOP is synchronized with CLK and it is responsible for stopping the coarse interpolator. Note that the counter input is determined by a multiplexer (controlled by MODE), thus the counter either counts clock edges in time-correlated operation or indi-

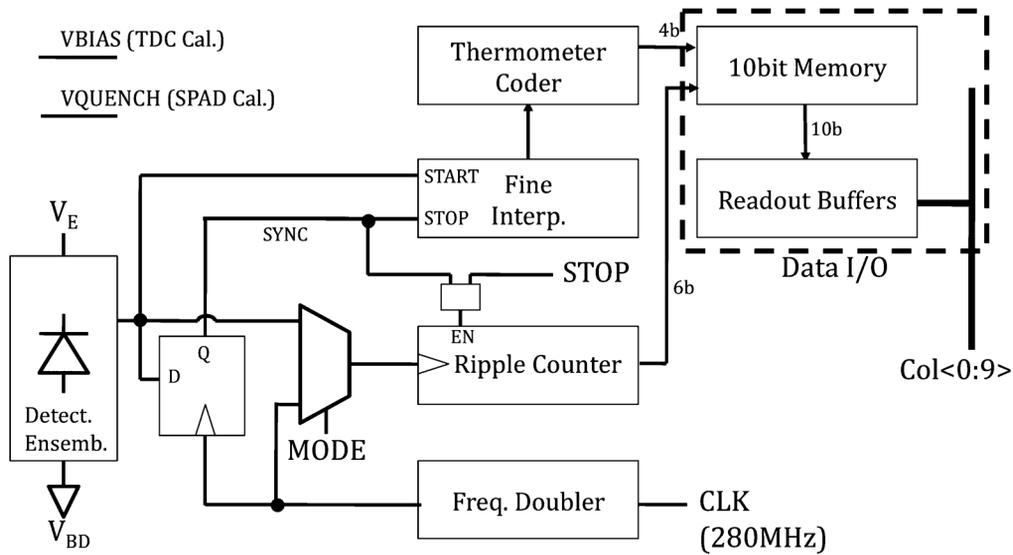


Fig. 5. Simplified block diagram of the pixel.

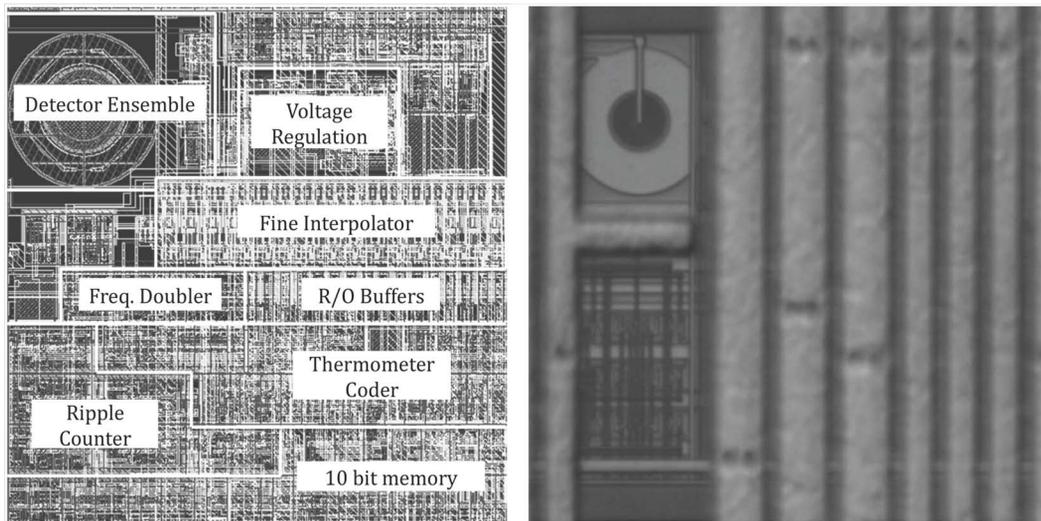


Fig. 6. Layout (left) and micrograph of the pixel (right).

vidual photons in time-uncorrelated photon counting mode. The layout and micrograph of the pixel is shown in Fig. 6.

III. SYSTEM ARCHITECTURE

A. Chip Architecture

With the pixel described previously, a time-resolved imager of 32×32 pixel array was designed and tested. For die size considerations the number of I/O pads is limited to two per column or 64 in total. As a consequence, the pixel array is divided into two sub-arrays of 16×32 pixels with each of the 32 columns having a dedicated I/O pad. The readout is performed using a rolling shutter approach. During the acquisition period, lasting $1 \mu\text{s}$, the data is collected and stored within the in-pixel memory, upon reception of the WRITE signal at the end of an acquisition window. During the subsequent acquisition period, the memory of each pixel is read out, while the pixel is acquiring new data. This scheme allows for continuous operation of the

entire array. In each sub-array the rows are read sequentially, starting from the center. The Y-decoder cell, driven by the external clock LINECLK, manages the readout by individually addressing each line of the two sub-arrays. The rolling shutter readout does not require any encoding of the pixel position, thus reducing the quantity of data that must be transferred out of the array. However, in the event of sparse photon detection, it is impossible to perform any data compression inside the sensor. The entire array can be read out in only $1 \mu\text{s}$, resulting in a 1 MS/s-pixel acquisition rate in time-correlated mode and a frame rate of 1 MHz in intensity imaging mode. A simplified timing diagram of the readout signals is shown in Fig. 7.

The frame starts with a WRITE signal asserted to transfer the content of the TDC acquired in the previous frame onto the memory. This allows us to perform a new acquisition while reading the previous one. The acquisition starts by resetting the TDCs and waiting for the first photon detection independently in each pixel. The data is transferred out of the pixels by a

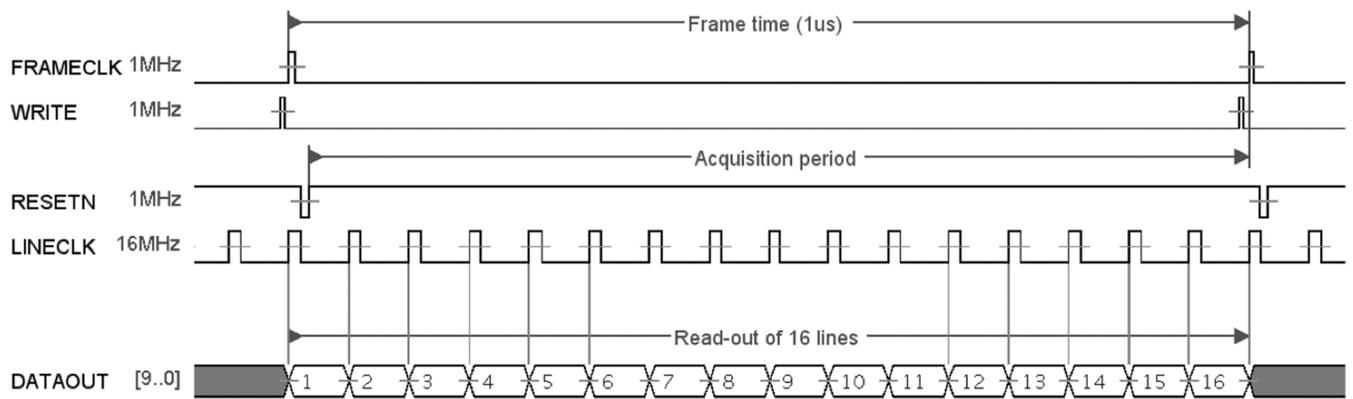


Fig. 7. Timing diagram of a frame acquisition. The total frame time is $1 \mu\text{s}$, the values stored within the pixel from the previous frame are read out in the subsequent frame. All 32 columns are read in parallel and all 16 rows in each half array are read sequentially.

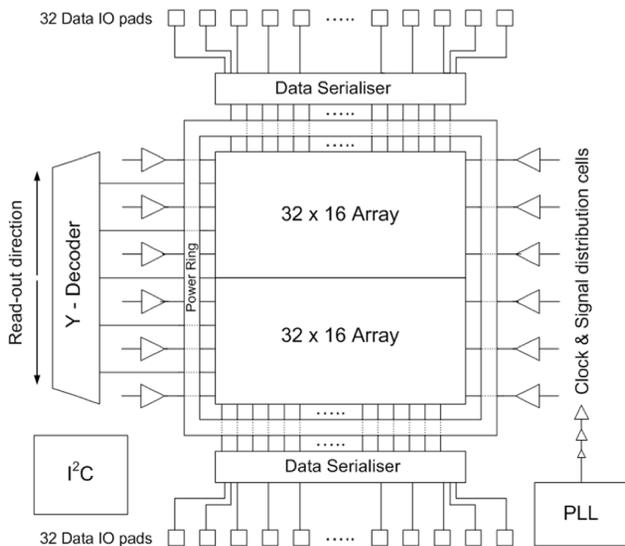


Fig. 8. Simplified schematic of the imager consisting of two sub-arrays each containing 32×16 pixels, data serialisers and a Y-decoder for readout as well as a PLL, clock trees and signal distribution cells.

10-bit wide data bus consisting of ten metal lines shared among the 16 pixels in the same column and same half array. Each of the pixels on the same bus has a tri-state buffer for each metal line; the buffers are activated by the Y-decoder, ensuring that only one pixel writes on the bus at any given time. There are, in total, the same number of data buses and I/O pads (64). As the data read by each 10-bit bus must be transferred out of the chip using a single pad, the data must first be serialised. 64 serialisers, one per sub-array column or semi-column, transfer the data to the I/O pads at 160 Mb/s. Serialiser circuits are standard, single-ended logic circuits that do not contribute significantly either to the digital noise or to the overall power consumption of the chip.

Fig. 8 shows a block diagram of the pixel array and the surrounding electronics handling the data and signal I/Os. With a 10-bit code being read out of each pixel every microsecond, the total amount of data generated by the imager amounts to $(32 \times 32 \times 10)/10^{-6} = 10.24 \text{ Gb/s}$. The on-chip PLL is used to drive the coarse interpolator of the in-pixel TDCs. The clock distribution is handled by clock trees injecting the clock from both the left and right sides of the array to minimize inter-pixel clock delays. A similar approach holds for all sensitive signals

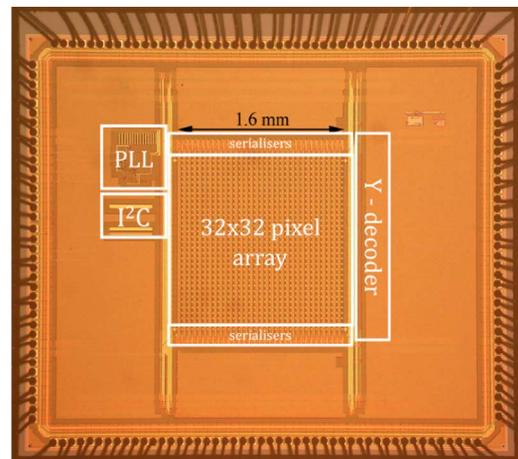


Fig. 9. Photomicrograph of the 32×32 pixel array. The chip dimensions are $4.8 \times 3.2 \text{ mm}^2$.

(START, STOP, etc.) distributed across the pixel array. A conventional power supply ring surrounding the pixel array distributes power in grid style so as to minimize localized IR drops that could have negative consequences to the accuracy of the TDCs. The internal grid was implemented using thick top-level metal, in some cases doubled by lower level metals. Each pixel was equipped with a decoupling capacitance to filter peak current consumption during high activity. Decoupling capacitances were also placed at the exterior of the array near the power ring. An I²C bus was integrated on the chip to control all operating modes and parameters, the PLL, etc. A complete chip micrograph is shown in Fig. 9.

B. Control and Data Management

The 32×32 pixel imager requires a number of control signals to operate. At the same time, the large amount of data generated by the imager requires a high-performance readout system capable of processing and storing the data. Both the control signals generation, data treatment, and storage are performed using a motherboard comprising two Virtex II-Pro FPGAs (Xilinx Inc., USA) that are organized as master and slave. The motherboard also contains multiple communication channels, amongst which two USB connections. A daughterboard provides the biasing and supply voltages for the chip and the appropriate connections between the imager and the motherboard.

The master FPGA is used to control the chip via an I²C bridge and to generate the operating and readout clocks. At the same time it retrieves the data generated by the chip. This data is immediately passed to the slave FPGA where it is processed and stored in the form of a histogram of photon arrival times for every pixel in the detector. Histograms were chosen to compress the data compatibly with FLIM. If we consider a histogram with 2^n bins, each bin consisting of a m -bit deep counter, the required memory size for a histogram H is $2^n \times m$. In our case, the TDCs yield 10-bit results, thus $n = 10$, while the counter depth m was chosen, for memory size considerations, to be 10, resulting in a memory requirement of 10,240 bits for a single histogram. However, the maximum possible number of TDC values V that can be stored within the histogram scales as 2^{n+m} . Thus, 2^{20} measurements can be stored in a single histogram. Without saving the data as histograms of arrival time, the same number of measurements would require $S = 2^{n+m} \times n$ bits of data. As a consequence, the compression ratio R is

$$R = \frac{S}{H} = \frac{2^{n+m} \times n}{2^n \times m} = \frac{2^{20} \times 10}{2^{10} \times m} = 1024.$$

Assuming a uniform data rate for all pixels, such a bandwidth reduction allows a lossless data transfer via USB. However, in real life applications, not all TDC output codes have the same probability of occurring, as the histogram reflects the optical waveform to be measured. As a result, those bins corresponding to the most likely TDC results will cause histogram saturation faster than expected, thus prompting a more frequent readout, potentially saturating the USB link. This issue calls for further work on data flow management that is beyond the scope of this paper.

Fig. 10 shows a column-wise segment of the firmware that manages the data from a single column. There are 32 such segments, while the section of the firmware that generates the controls for the sensor chip is shared among all segments. The data is read out serially from the SPAD array, deserialised, and fed to a data snooper that converts the 32×10 -bit format for the lower and upper rows onto 8 packets of 10-bits. This deserialisation procedure is actually the bottleneck that limits the speed of the system to 500 kfps, as mentioned earlier. The packets are distributed onto 8 memory spaces shared among 4 pixels. Each pixel is associated to a single reduced histogram comprising 128 10-bit bins of 119 ps each. When a new non-zero TDC measurement hits the snooper the bin of the histogram of the corresponding pixel is incremented, up to 1024 counts, at which point the histogram is blocked to prevent distortion. When the main controller receives an acknowledgement signal, the entire histogram content is transferred via the USB bridge to a PC. The PC can thus extract the appropriate parameter, e.g., the lifetime of a single-exponential fit, and display it in real time for each pixel.

IV. CHARACTERIZATION

The scaling from a single detector and its electronics to a moderate or large array of pixels is associated with a number of issues: local power consumption, digital noise, overall heating, and process non-uniformity, to name the most critical ones. The

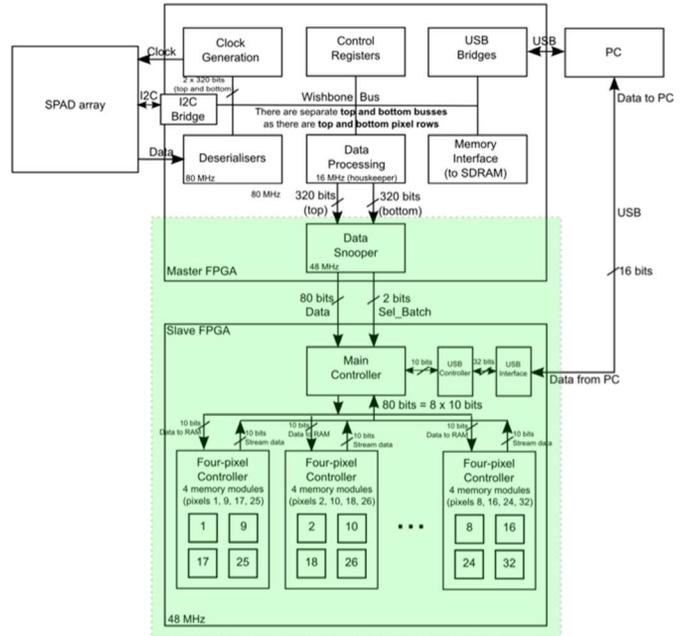


Fig. 10. Firmware block diagram.

characterization of the sensor described in this paper, denominated MF32, has been performed at two levels. First, the pixel performance is characterized in terms of individual SPAD and TDC parameters. Second, the overall sensor performance and non-idealities are characterized due to doping non-uniformity and lattice defects, such as traps, dislocations, and other lattice damages.

For the present imager, maps of the dark count rate (DCR) across the array at room temperature are given for two excess bias voltages. Fig. 11 shows a spatial map of DCR and Fig. 12 plots the cumulative distribution of DCR across all the pixels. For an excess bias voltage of 1 V, the median DCR is only 100 Hz, or 4 Hz/ μm^2 , a relatively low noise level if compared to other CMOS SPADs but higher than that of SiPMs built in dedicated technologies. A distinct increase of DCR is noticeable around 1.5 V of excess bias, this has dictated the choice of 1 V for our experiments. While the cause of this sudden increase in DCR cannot be identified with certainty, it is likely to be induced by the breakdown of secondary junctions unrelated with the active region of the SPAD. In these tests, VQUENCH was set so as to achieve a dead time of 100 ns, which was selected to reduce afterpulsing probability below 0.1%.

The DCR of the SPAD array compares very favorably with other deep-submicron detector implementations [17], [20], [21] and even with other SPAD arrays implemented in older technologies such as [8], while it is generally higher than implementations in dedicated technologies that are optimized for noise. However, as is the case for all CMOS SPAD implementations, the active area of the detector is kept relatively small to ensure an acceptable DCR on a high number of pixels. With an active area of $\sim 50 \mu\text{m}^2$ for a total pixel array of $2500 \mu\text{m}^2$ the fill factor does not exceed 2%. To mitigate this limitation, an array of microlenses based on a design described in [22] was used. The achieved concentration factor was characterized over all

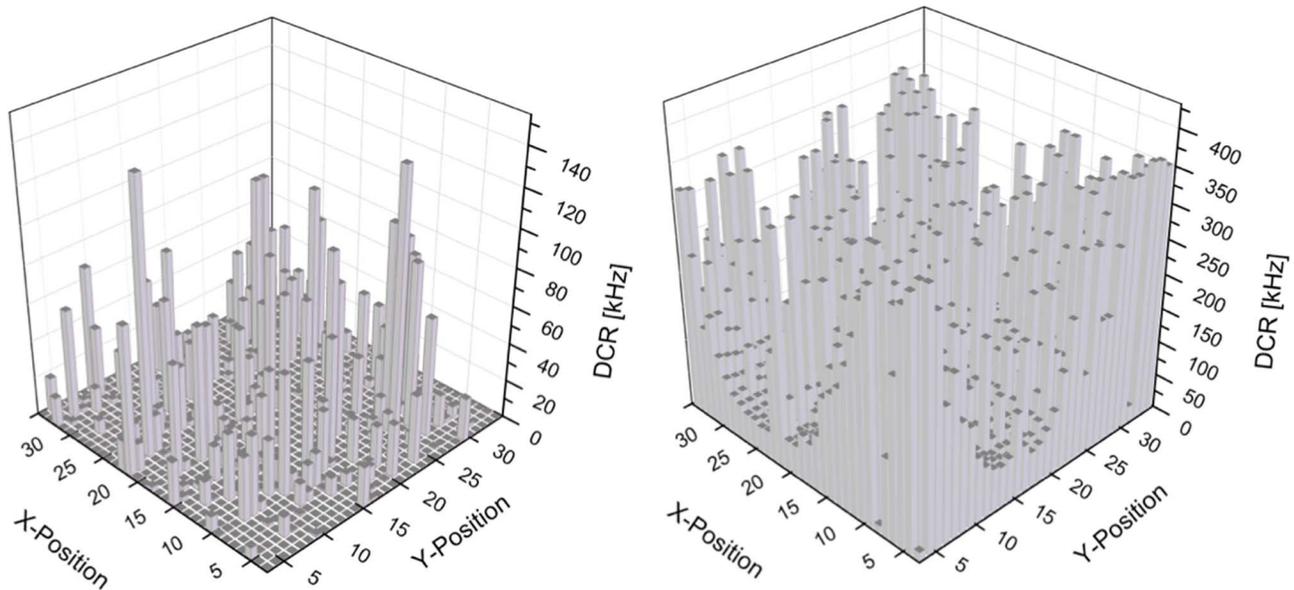


Fig. 11. DCR distribution across the 32×32 pixel array for 1 V (left) and 2 V (right) of excess bias voltage.

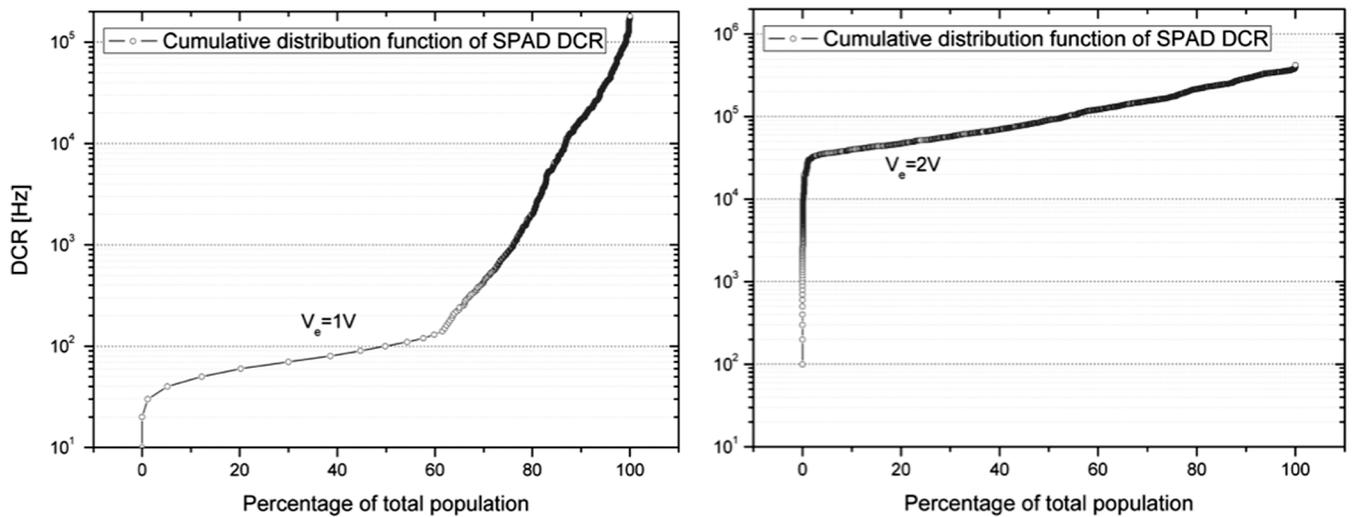


Fig. 12. Cumulative distribution function of the DCR within the array for 1 V (left) and 2 V (right) of excess bias voltage. The median DCR is 100 Hz and 90 kHz, respectively. The measurements were conducted at room temperature.

pixels and has shown strong variability across the array with a median of approximately 5, thus enabling an effective fill factor of approximately 10%.

SPAD crosstalk is an effect by which a pixel detecting a photon, or a dark count, may affect the likelihood of a neighboring pixel to generate a count. The macroscopic effect is blurring. The sources of crosstalk are optical and electrical. For details on optical crosstalk, see [23]. In the present detector array, the SPADs are placed within a deep n-well, isolating them from the bulk silicon and thus highly reducing the probability of electrical crosstalk. Furthermore, the integration of quenching electronics at pixel level significantly reduces the quenching time and the amount of carriers crossing the diode, which in turn decreases the probability of optical crosstalk. We computed the cross-correlation function between the outputs of all adjacent pixels pair-wise, a technique used successfully in [24]. The absence of correlation between adjacent pixels indi-

cates that negligible crosstalk (electrical or optical) is detected. TDC crosstalk was minimized by careful design and layout that prevented IR drops, that in turn would cause resolution variability due to variable propagation delays. Switching noise was also minimized by placing a large matrix of local decoupling capacitances. The interference due TDC operation was measured by activating a variable number of TDCs by acting on illumination levels. The results of this analysis are in the performance summary.

The pixel timing performance was assessed optically using an excitation of a pulsed laser source (Advanced Laser Diode Systems GMBH, Germany) emitting short (< 40 ps) light pulses at a frequency of 40 MHz. The source was also operated at frequencies as low as 2 MHz, while higher frequencies (up to 80 MHz) have also been successfully tested. The START signal of the TDC was triggered upon photon detection by the SPAD while the STOP was given by the laser's electrical synchronization

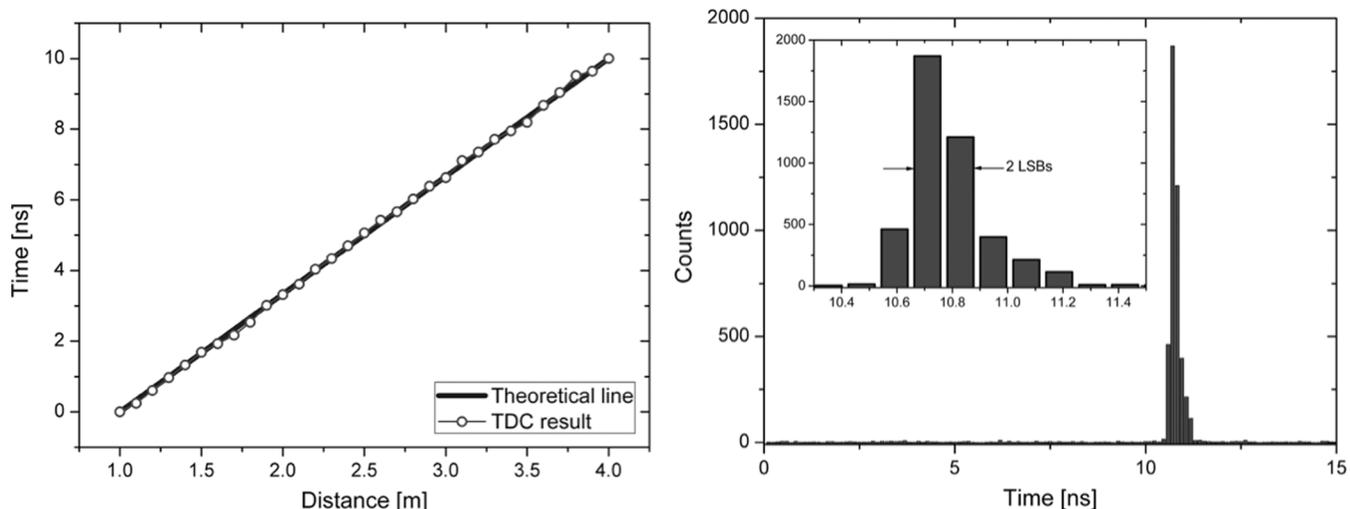


Fig. 13. TOF measurements vs. theoretical delay for different laser-to-chip distances (left); typical histogram for repeated TOF measurements with a constant delay for 5000 samples (right). The computed TOF error (1 σ) is less than the standard deviation of the Gaussian fit of the histogram for the same number of samples.

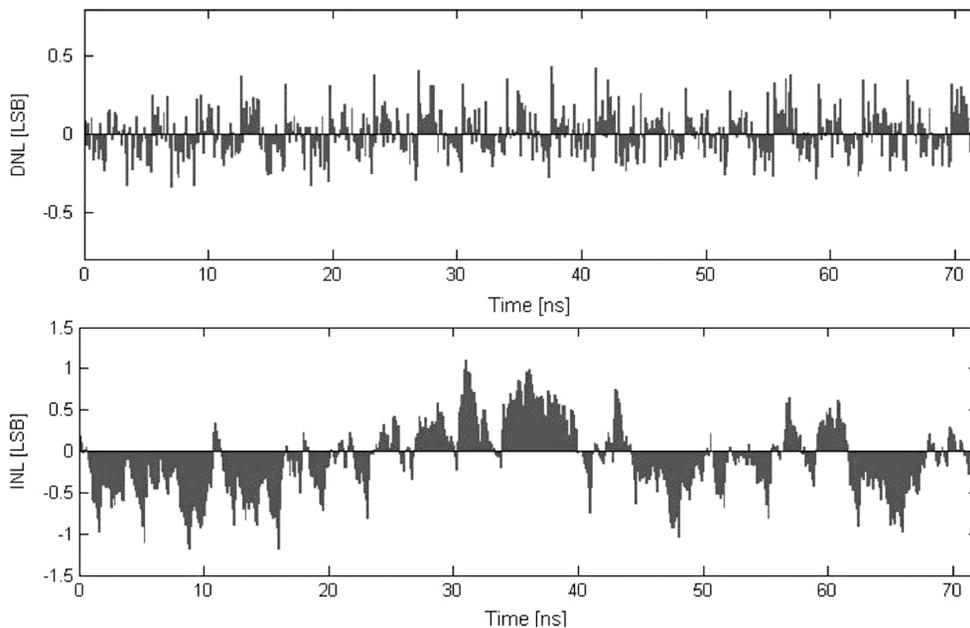


Fig. 14. Measured DNL and INL with a timing resolution (bin width) of 119 ps at room temperature. The DNL was achieved by use of a density test with uniform illumination, a standard procedure in the literature of TDC testing.

pulse. The time-of-flight (TOF) of the laser pulse can be measured in this fashion, while the accuracy of the TDC can be assessed by changing the laser-to-sensor distance. The timing accuracy of the entire system comprising the laser (17 ps of timing jitter), SPAD (61 ps) and TDC is 101 ps (or 2 LSBs). Assuming that the jitter is a random process resulting from statistically independent sources (SPAD, TDC, and laser), its standard deviation σ_{TDC} can be estimated as $\sigma_{\text{TDC}} = \sqrt{101^2 - 61^2 - 17^2} = 78.5$ ps or 185 ps FWHM. Fig. 13 shows the measured time delay for a laser-chip distance of up to 3 meters with the theoretical delay shown as reference value as well as the typical histogram obtained when repeating the measurement for one specific distance.

The DNL and INL of the TDC were evaluated through a density test using uniform, diffused wideband light illumination of the array, so as to achieve a uniform time-of-arrival of photons

impinging upon the array. A histogram of photon arrival times and the DNL was obtained by dividing the result of each bin of the histogram by the average result over all the bins in the histogram. Then, the INL was calculated by integrating the DNL. The DNL and INL were measured in a range of ± 0.4 LSB and ± 1.2 LSB respectively, with a bin width of 119 ps. The results are shown in Fig. 14.

In fluorescence lifetime imaging, where the image contrast is given by the timing information rather than the photon count, it is most important to ensure good uniformity of photon timing across the pixel array. Failure to do so would result in a steady offset at specific locations within the image, much like fix pattern noise in conventional imagers. With the large pixel array area ($1600 \times 1600 \mu\text{m}^2$) and the high number of signal and power lines running across the device, non-uniformity of the timing information can be significant. In the present device

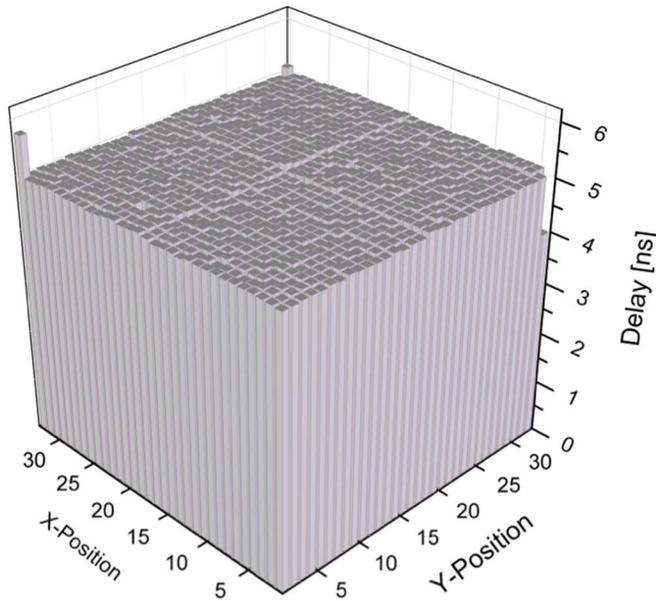


Fig. 15. Bar plot of the pixel uniformity measurement across the full pixel array.

the use of a global PLL-generated clock as timing reference for the coarse TDC interpolator ensures good uniformity of the coarse measurement. In the case of the delay line, local variations could not be compensated for due to pixel area restrictions. However, the short operation range (1.79 ns) should limit the effect of delay-line non-uniformity over the entire measurement. The uniformity of the array was assessed by a shining a short (<40 ps) laser pulse with repetition rate of 40 MHz on the pixel array. For each pixel, the resulting histogram was fitted to a Gaussian curve and the maximum of the Gaussian curve was plotted in Fig. 15. The result shows very uniform TDC results across the entire array, except for the separation between quadrants due to the partitioning of the clock distribution networks. In applications such as FLIM though this non-ideality is unimportant as it is systematic and can be easily suppressed by calibration.

With the imager being divided in two sub-arrays (see Fig. 8), a slight offset can be recognized at the interface between the top and bottom array. A similar discontinuity was observed at the interface where the clock signals, distributed from the right and left side of the array, meet. Fig. 16 depicts the uniformity across all pixels, arranged in a line, for two different time intervals (~ 5.2 ns and ~ 15.0 ns). The standard deviation across the pixels is 67 ps and 44 ps respectively. In the shorter time interval measurement, 90% of the range of the fine interpolator is used whereas the SPAD pulse only travels through 40% of the delay line in the longer time interval. The difference in the usage of the delay line is the most likely explanation for the discrepancy in standard deviation between the two measurements. The plot also evidences the effects of using two separate clock distribution networks from the sides to the middle of the chip.

With the integration of the highly scalable pixel into a 32×32 pixel array, the possibility of integrating even larger time-correlated imagers is largely dependent on power consumption. The suitability of the architecture for larger array integration was verified by measuring the current dissipation trends with

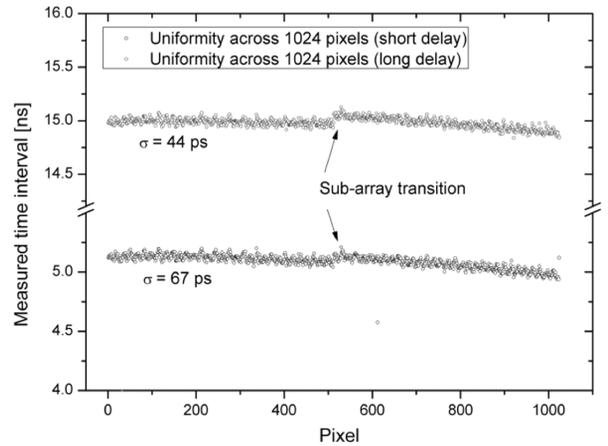


Fig. 16. Uniformity of the TDC measurements for two different time intervals. A slight discontinuity is observable at the interface between the top and bottom half-arrays.

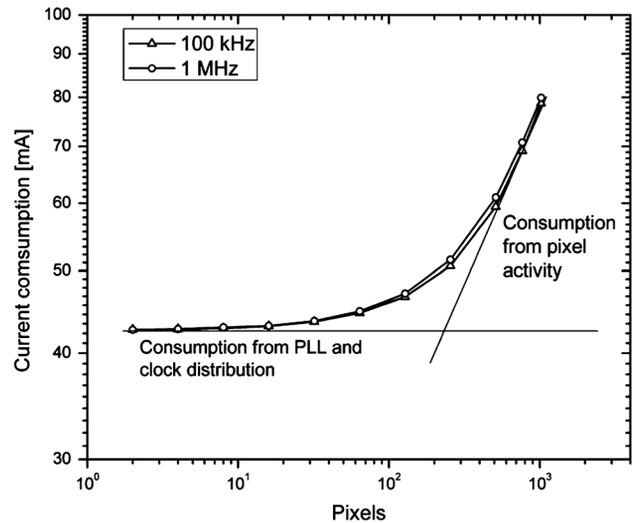


Fig. 17. Core current consumption (without I/O) at 1.2 V supply for two photon detection rates.

increasing numbers of active TDCs as shown in Fig. 17. A globally generated clock was preferred over a local pixel-level clock to reduce the power dissipation in the pixel to a minimum, at a cost of increased off-pixel power dissipation. Furthermore, since the TDCs are event-driven (triggered by the SPAD), the power consumption is lower for low illumination levels, whereas the noise of the detector, due to local heating, is also minimal. When few pixels are enabled, the power consumption is dominated by PLL and clock distribution. With an increasing number of activated pixels, in-pixel power dissipation becomes dominant. From Fig. 17 we can conclude that the PLL and clock distribution absorbs 42 mA while the entire chip at maximum activity 78 mA. The main characteristics of the individual pixel and of the full array are summarized in Table I. The sensitivity and wavelength spectral range of the SPAD in this paper are identical to [25] that reports on the same detector implemented in this sensor.

The device was demonstrated for FLIM in a wide-field optical setup shown in Fig. 18. The optical setup takes full advantage of the parallelism offered by the 1024 FLIM acquisition channels and enables one to acquire a full image in real time. The imaging setup consists of a pulsed laser source emitting short

TABLE I
PERFORMANCE SUMMARY OF THE MEGAFRAME PIXEL ARRAY. ALL MEASUREMENTS WERE PERFORMED AT ROOM TEMPERATURE

Performance		Min.	Typical	Max.	Unit
System	CMOS Technology		130nm		CIS
	Format		32x32		-
	Pitch		50		μm
	Fill Factor		2		%
	Resolution (LSB)		119		ps
	Temporal Jitter (FWHM)		185		ps
	DNL/INL			$\pm 0.4/\pm 1.2$	LSB
	Non-Uniformity (std. dev.)		67		ps
	Range		100		ns
	Sampling		500	1000	kS/s-pixel
	Power (Core Only)		90		mW
Pixel	DCR @ 1V Excess (median)		100		Hz
	SPAD Intrinsic Dead Time		100		ns
	SPAD Photon Detection Probability @ 1V excess	5		25	%
	Wavelength Range	350		850	nm
	Afterpulsing			<0.1	%
	Crosstalk @ <20% of active TDCs			<0.1	%

TABLE II
COMPARISON WITH OTHER STATE-OF-THE-ART IMAGE SENSORS

	[6]	[7]	[8], [27]	[18]	[26]	[28]
CMOS Technology	0.8 μm	0.8 μm	0.35 μm	130nm CIS	130nm CIS	180nm CIS
Format	32x32	64x1	128x128	32x32	32x32	32x1*
Time-of-Arrival Measurement	External TDC	In-Pixel TAC & Analog Counter	Column-level TDC (32)	In-Pixel TDC	In-Pixel TAC & Analog Counter	On-chip TDC (32)
Pitch [μm]	58	38 (Linear)	25	50	50	50 (Macro)
Fill Factor [%]	1.1	13 (Linear)	6	2	2	70 (Linear)
Resolution (LSB) [ps]	120	50	70	52	160	208
Temporal Jitter (FWHM) [ps]	300	-	230	0.6LSB**	600	-
DNL/INL [LSB]	-	-	$\pm 0.25/\pm 0.1$	$\pm 1.4/\pm 0.4$	0.7/1.9	0.52/0.73
Non-Uniformity	1%	3%	-	8LSB	± 2 LSB	-
Range [ns]	25	-	100	55	20	420
Sampling [kS/s-pixel]	-	10	19	500	500	12,500
Power [mW]	100	1 (Core Only)	150	38	300	-

*) Each macro-pixel comprises 6x2 SPADs; **) Mean value for TDC only.

(<40 ps) light pulses at a frequency of 40 MHz at a wavelength of 405 nm with an mean power of 2 mW (Advanced Laser Diode Systems GmbH, Germany). The laser beam is then directed into a fluorescence microscope (BX51IW, Olympus, Japan) where a dichroic beam splitter cube redirects the beam to the microscope objective (20x, 0.45 NA, MPlanFL N, Olympus, Japan) and to the sample. The fluorescent light emitted by the sample is captured by the same objective and sent through the dichroic beam splitter, which filters out backscattered laser light, to the SPAD array. Time discrimination is performed on-chip using the in-pixel TDCs in reversed start-stop configuration. The stop signal is given by the lasers reference signal and the start by the SPADs. The fluorescence lifetime data is collected and stored as an individual histogram for each pixel on the motherboard.

Finally, the collected data is read out to a personal computer through a USB link.

The instrument response function (IRF) of the system is characterized in Fig. 18 and was measured to 380 ps FWHM. The sample used for the wide-field FLIM acquisitions is a mixed pollen grain slide (Carolina Biological Supply Company, NC, USA) containing a mixture of pine, sunflower, cattail, alnus, evening primrose and lily pollen. The bisaccate pollen grains studied in detail in this section were stained with either Harris hematoxylin and fast green, or Harris hematoxylin and phloxine.

Fig. 19 depicts wide-field FLIM acquisitions with a resolution of 30×32 pixels of the pine pollen grain. Fitting of the time-correlated fluorescence data was achieved with the help

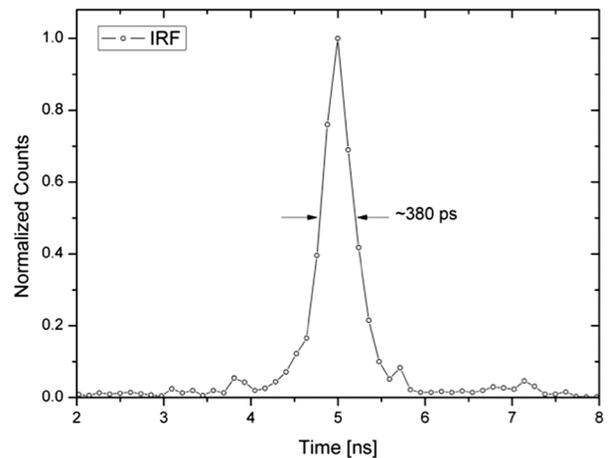
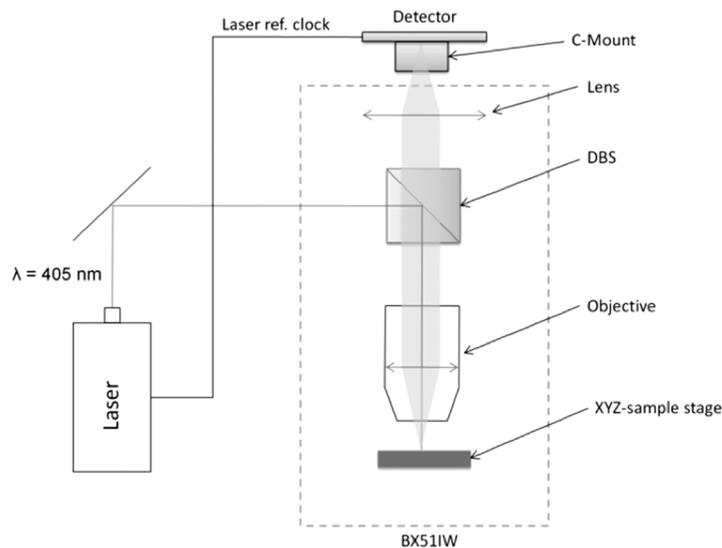


Fig. 18. Optical setup used in the experiments (left). Instrument response function of the system (right).

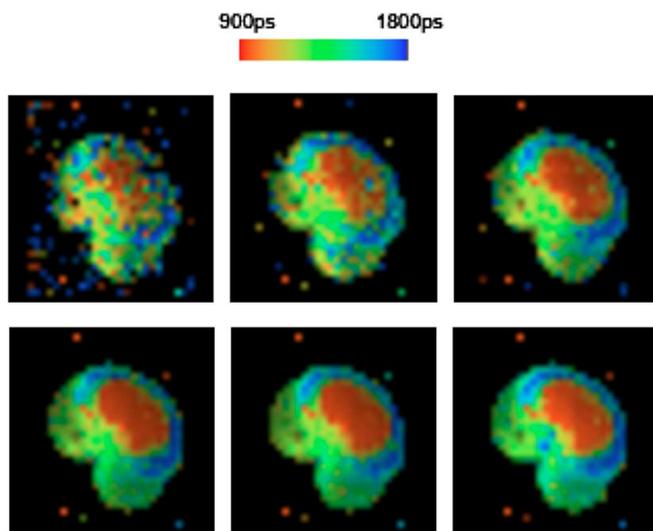


Fig. 19. FLIM image of a bisaccate pollen grain. The pollen was stained with two fluorophores binding with different regions of the organism. The fluorophores have distinct lifetimes and can therefore be selectively observed. The panel sequence shows the results of exposing the sample for 69 ms, 73 ms, 130 ms, 254 ms, 454 ms, and 566 ms (from top left to bottom right), respectively. The false colors represent the range of lifetimes estimated by the method.

of the SPCImage software (Becker & Hickl GmbH, Germany). A double-exponential fit was found to best suit the data. The contrast of the images is given by the weighted average of the lifetime components. The two “sacs” or bladders facilitate wind dispersal of such grains and yield a significant lifetime contrast in the FLIM images depicted in the figure. The histogram of the response in one pixel and the exponential fit are shown in Fig. 20 for an exposure of 566 ms. During this exposure a theoretical maximum of 283,000 time-of-arrival measurements could be achieved independently in each pixel. However, due to the photon-starved nature of the illumination regime, only a fraction of measurements actually yielded a viable value, though sufficient for a high-quality FLIM image.

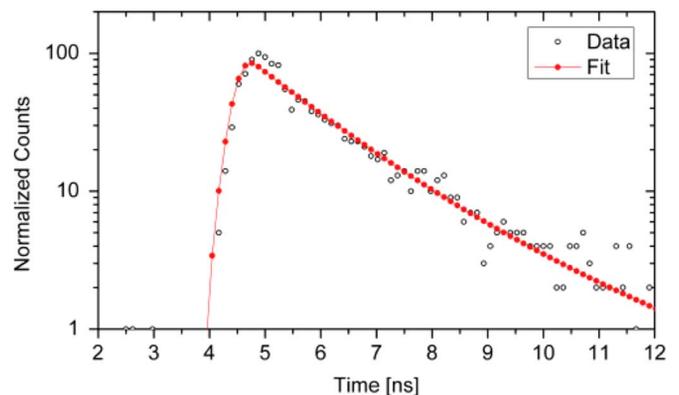


Fig. 20. Histogram of the TCSPC response at 566 ms overall exposure. In this plot one can recognize the exponential decay of the response observed by a pixel and the fit that is performed on such response. From the lifetime extracted from the fitted response one can ascertain which fluorophore(s) has/have caused it.

V. CONCLUSION

A sensor was presented capable of detecting single photons over an array of 32×32 pixels, simultaneously evaluating their time-of-arrival with a resolution of 119 ps and a 10-bit range. With a median dark count rate of 100 Hz and highly uniform sensitivity, the detector is very well suited for photon-starved applications such as fluorescence lifetime imaging microscopy and it compares favorably in this respect with the literature (see Table II). Thanks to a timing uniformity better than 2 LSB, fluorescence lifetimes can be recorded precisely on up to 1024 channels, each operating at up to 1 MS/s independently. The very large quantity of data (10 Gbps) produced in time-correlated operation mode is handled by an effective histogram-building firmware running on commercial Virtex-II Pro FPGAs. Finally, the use of deep-submicron CMOS technology and event-driven pixel operation make the imager highly scalable, opening the way to even larger implementations and higher performance.

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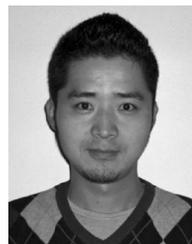
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