The Gigavision Camera
A 2Mpixel Image Sensor with 0.56μm^2 1-T Digital Pixels

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Abstract – *We present a CMOS image sensor with deep-subwavelength, digital 1-T pixels designed for use in a digital film concept known as Gigavision (GV) camera. In GV, the levels of gray in the picture are derived from the concentration of activated pixels. Activated pixels are pixels hit by one or more photons. The advantage of this approach is a predictable, highly uniform logarithmic response, thus enabling high dynamic range images. Applications include automotive and environmental monitoring, HDR vision, etc.*

In the GV concept, inspired by [1], the pixels are organized in programmable overlapping clusters. Thus the concept of a fix-size pixel evolves into one whereby the boundaries of the pixel may extend to the entire array with a proper but weighted differently, locally. In GV, the image is reconstructed through an optimization process that involves all the pixels of the camera, thus mimicking the continuous, global effects of the lens [2].

Fig. 1 shows the overall GV concept. The image reconstruction by external software algorithm is done in a programmable matrix in a way that allows anti-aliased grayscale images, thus increasing image quality and achieving a reproducible, high dynamic range imager [3].

To realize a deep sub-wavelength pixel, we propose a 1-T pixel structure with three states [4]. A schematic diagram and potential diagrams of the pixel are illustrated in Fig. 2. During the accumulation state, the gate voltage is biased at low voltage to accumulate photoholes generated into the floating body. Electrons are simultaneously drained to the drain. Medium voltage is used during the readout state to transfer the accumulated holes to the source region without any residual holes. Finally, the gate is biased at high voltage to reach the reset state.

Simulation results, obtained with SPECTRA [5] are shown in Fig. 3. Accumulation and transfer time were set to 10ns to reduce simulation times. Holes are effectively accumulated in the p-region at gate voltage 0 or 0.2V even in this short accumulation time. During the readout state, the accumulated holes are transferred to the source region, but perfect transfer is only achieved in longer time intervals. The reset state is achieved properly in the simulation. In Fig. 4 the theoretical response of the GV sensor is plotted as function of impinging photo intensity for different values of pixel oversampling and of activation threshold [2].

A CMOS image sensor comprising an array of 1600 × 1200 pixels was fabricated in a standard 90nm CMOS process. A microphotograph of the chip is shown in Fig. 5. The die size is 2mm × 2mm and the unit pixel pitch is 0.75μm. Half of pixels were combined to a fully digital readout architecture; the other half can be read out with a conventional analog architecture for test purposes.

Fig. 6(a) shows the analog signal path. The circuit comprises analog biasing, amplification, and S&H circuitry. Fig. 6(b)

shows the digital signal path. It comprises a sense amplifier and latching circuitry similar to the readout circuitry of a RAM. The specifications of the chip are summarized in Tab. 1.

References

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[2] L. Sbaiz, F. Yang, E. Charbon, S. Süsstrunk, M. Vetterli, "The Gigavision Camera", Intl. Conf. on Acustics, Speech and Signal Processing (ICASSP), 1093-1096 (2009).

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[5] H. Mutoh, "3-D Optical and Electrical Simulation for CMOS Image Sensors", IEEE Trans. on Electron Devices, **50**(1), 19-25 (2003).

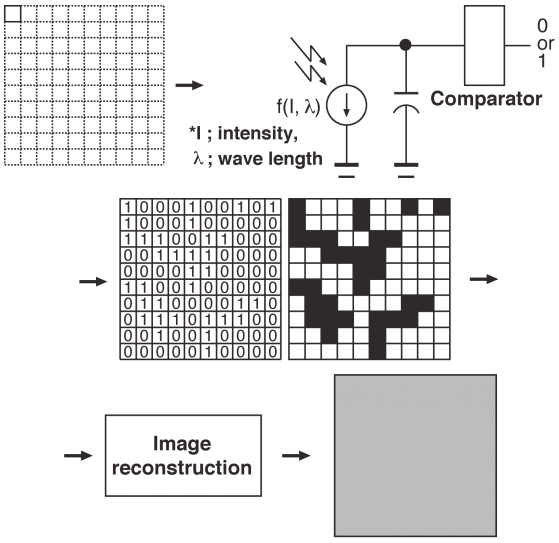

Fig. 1. Concept of the Gigavision camera: highly miniaturized pixels with digital output. Gray levels are obtained from the distribution of "1" and "0" pixels over the entire array by an optimization algorithm that enables virtually aliasing-free, high dynamic range images.

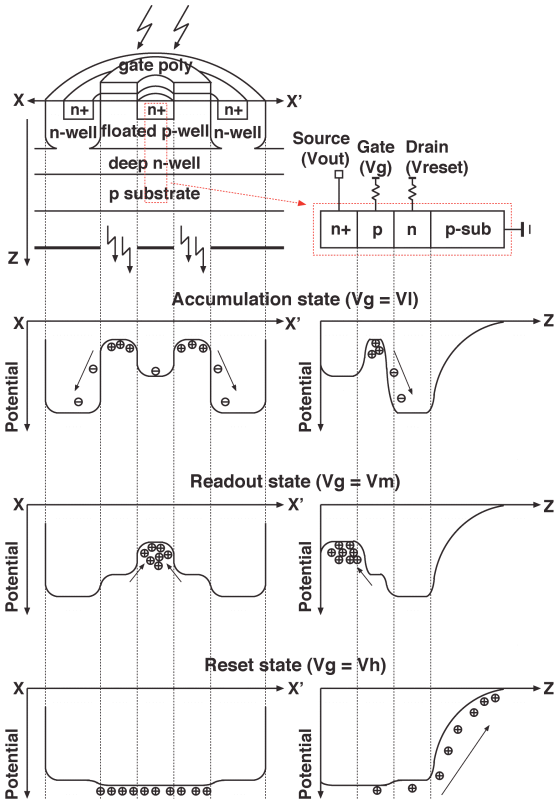

Fig. 2. Schematic and potential diagrams of a pixel. The pixel has 3three operating states (accumulation, readout, reset) achieved by proper biasing of the gate using a vertical shift register with voltage controller.

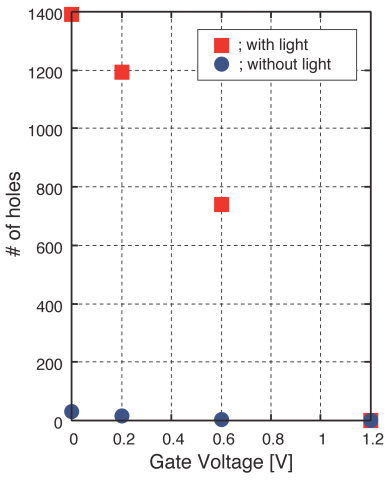

Fig. 3. Simulated response of the pixel with two exposure situations. Both integration and transfer time were set to 10ns. Light power and wavelength were set to 10W/cm^2 and 550nm, respectively.

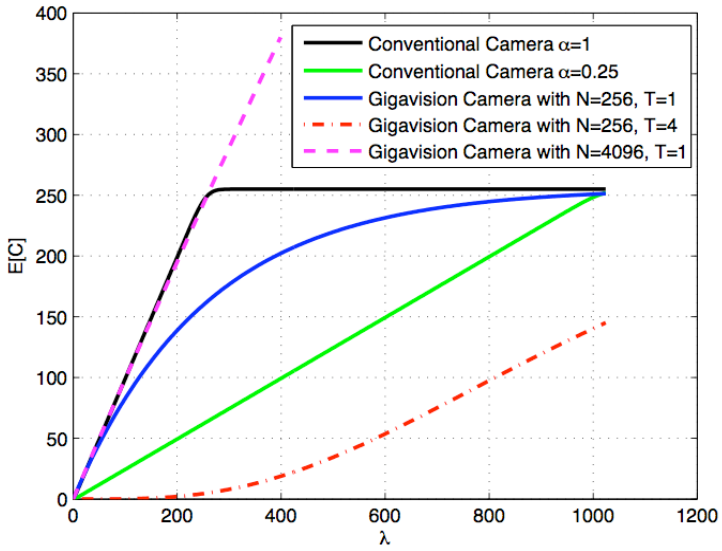

Fig. 4. Theoretical response of a GV pixel for different sizes of pixel oversampling factor N, and threshold levels T. The threshold level indicates the minimum number of photons that cause a pixel to switch from "0" to "1" state.

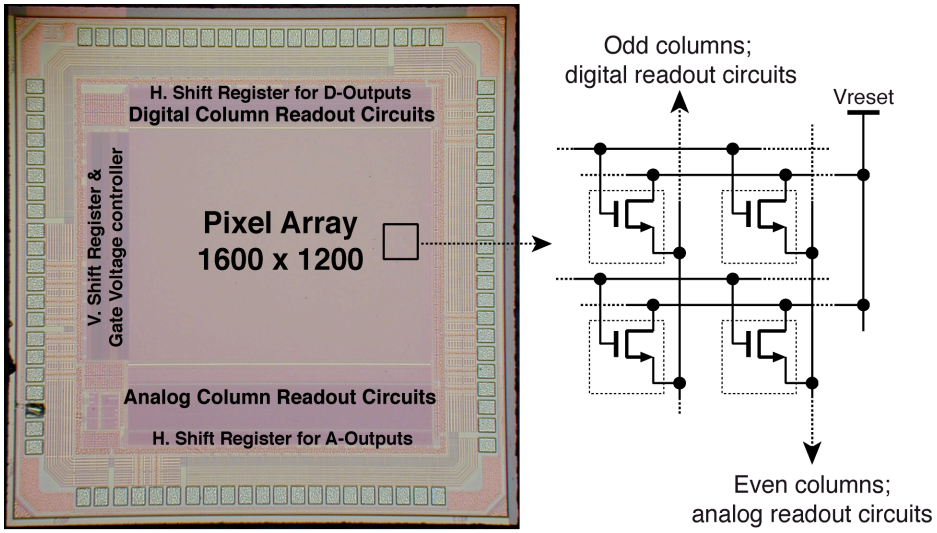

Fig. 5. Chip micrograph. Even columns of pixels are used for analog readout and odd columns are read out by the digital readout circuit. The die size is 2mm × 2mm and the unit pixel size is 0.75µm × 0.75µm. A 1poly-9metal 90nm CMOS standard process without microlens is used for this design.

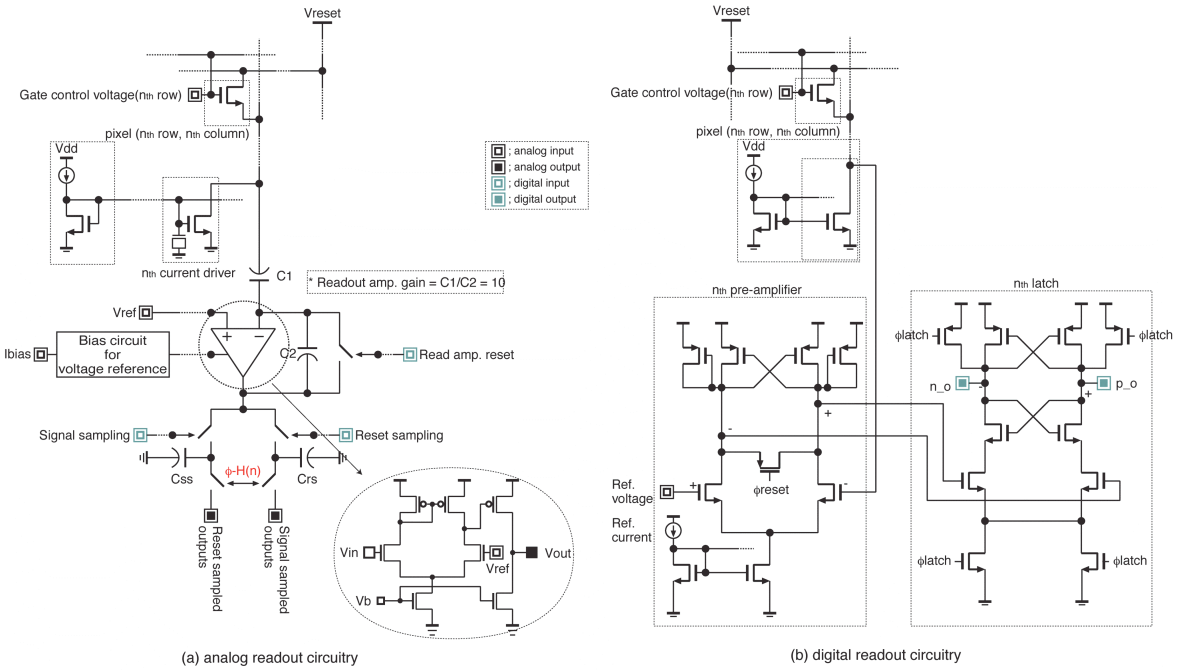

Fig. 6. (a) Analog readout circuitry. Internal readout gain for analog readout was set to 10. Analog output is reprocessed by external commercial ADC with 14bits. Both amplifier speeds are designed at 30MHz for video rate speed. (b) Digital readout circuitry. The signal path comprises a sense amplifier and it is similar to a digital RAM readout circuit.

Parameter	Value	Comments
Process	90nm 1P-9M standard CMOS	Without microlens array & color filters
Chip Size	2 x 2 sqmm	
Pixel Size	0.75 x 0.75 sqμm	1-T structure
# of Pixels	1600(H) x 1200 (V)	With digital & analog column readout
Supply	1.2V	Pixel / readout single supply

Tab. 1. Summary of specifications of the chip.