Poisson Distributed Noise Generation for Spiking Neural Applications

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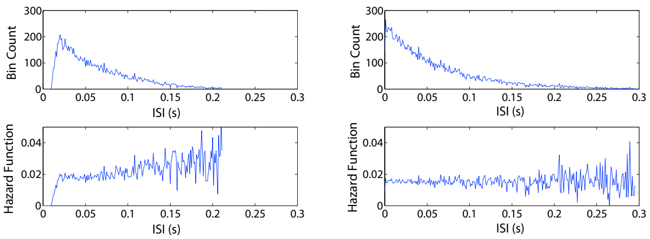
***Abstract*— Poisson distributed spike trains are often used as the input to VLSI implementations of spiking neural networks. However, it can be difficult to generate large truly random spike distributions which can be easily applied as input to a chip. This work presents results recorded from an avalanche photo diode which demonstrates that it can be used to create a Poisson distributed spike train and describes the circuitry which will allow it to interface with other neuromorphic chips using the Address Event Representation protocol. The chip is currently being fabricated using the AMS 0.35μm HV process.**

I. Introduction

Noise is generally regarded as undesirable, but within neural networks it is often beneficial. Probabilistic structures such as the Continuous restricted Boltzmann Machine (CRBM) [1] require noise to operate, and Fusi et al. [2] show that stochastic synaptic plasticity can increase a network's learning and remembering potential. At the individual neuron level, recorded cell data from a randomly firing neuron exhibits statistics very similar to a Poisson distributed noise source. Figure 1 shows the inter-spike interval (ISI) distribution and hazard function of data recorded from a VMH neuron which has been classfied as randomly firing and a matlab generated Poisson distributed noise source.

A hazard function shows the probability of a spike event being generated at a given time interval since the previous event, given that a subsequent event has not yet occurred. A purely Poisson distributed process has a constant probability of producing an event irrespective of the time since the previous event, which is shown as a flat distribution. The recorded neuronal pattern is similar to the matlab generated data, except for a refractory period immediately subsequent to a spike event.

If it is desirable to include a noise source, it can be difficult to create one with the required characteristics. Alspector et al. [3] report that while amplifying the thermal noise of a resistor was a good source of noise, high frequency oscillations cause the noise generators to correlate. An alternative technique that does not suffer from correlations, and was suitable for VLSI implementation, is presented in [4]. If spiking noise is required, Chicca and Fusi show how a randomly connected recurrent network can be used to generate a stochastic spike train [5]. A review of other techniques can be found in [6].



(a) (b)

Fig. 1. The inter-spike interval (ISI) in one ms bins and hazard function of (a) data recorded from a randomly firing cell and (b) a matlab generated Poisson spike train.

This work focuses on creating a noise source for a spiking neural network implemented in analogue VLSI. A method for generating a Poisson distributed spike train is introduced. The source of the noise is the dark count from a single photon avalanche diode (SPAD). An array of these detectors is created with Address Event Representation (AER) readout circuitry [7] which will allow it to interface with other neuromorphic chips.

Section II introduces the avalanche photo diode used. Recordings showing the noise characteristics of the photo diode are presented in section III. The circuitry contained in the array is described in section IV, and the paper ends with conclusions and a discussion on future work.

II. Single Photon Avalanche Diodes

The concept of the avalanche photodiode was first proposed by Haitz et al. [8]. In recent years much work has focused on implementing single-photon avalanche diodes in a standard CMOS process [9], [10], [11]. SPADs realised in a foundry CMOS process were first demonstrated by Rochas et al. in

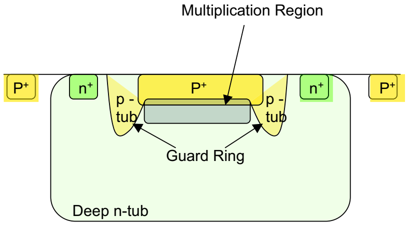


Fig. 2. The structure of the SPAD device.

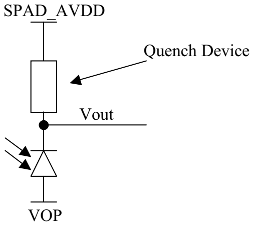


Fig. 3. The SPAD with quench resistor

2002 [12]. If biased above breakdown, the gain of a SPAD approaches infinity, thereby ensuring Geiger mode operation. The SPAD is biased such that upon detection of a single-photon a transistor-transistor logic (TTL) compatible pulse is produced.

The SPAD detector implemented in this project consists of a circular dual junction structure: p+ anode/deep n-well/p-substrate (Figure 2). The p+ anode/deep n-well junction forms the avalanche multiplication region where the Geiger breakdown occurs. The n-well/p-substrate junction allows the p+ anode to be biased independently from the substrate and prevents electrical cross-talk. A p-well guard-ring surrounds the p+ anode to prevent premature breakdown [13]. The device has a diameter of 6μm resulting in an active area of 28.27μm^2.

A diode biased beyond its reverse bias breakdown voltage will remain in a non-broken down state (zero current flowing) for a relatively long period of time (in the order of milliseconds). It is the occurrence of a primary free carrier within the high electric field p-n junction that triggers an avalanche breakdown event.

When operated as a photo-detector it is always hoped that this primary free carrier is generated as a result of an incident photon. However, spurious breakdown events do occur due to thermal or tunnel generated carriers and trapped charges.

If a free electron-hole pair is generated within the depletion region of the p-n junction, the high electric field caused by the large reverse bias voltage, will accelerate the electrons and holes towards the p and n regions respectively. The accelerated free electron and hole collide with static electron-hole pairs in the junction, resulting in impact ionization. These newly created free electrons and holes are subsequently accelerated, resulting in further collisions and hence ionization events. As the number of free electrons increases, so does the current flowing through the SPAD device. The number of free electron-hole pairs, and hence current, continues to rise exponentially until quenching occurs.

In order to ensure the SPAD detector's compatibility with standard CMOS circuitry, the biasing of the SPAD must be carefully considered. The logic levels of the 0.35μm process used in this project were 0V (logic 0) and 3.3V (logic 1). Therefore, it had to be ensured that the output transition of the SPAD on breakdown had a 3.3V swing. This is achieved by setting up appropriate bias conditions. For the SPAD to operate in Geiger mode it must be biased above its breakdown voltage. The p+ anode of the SPAD is therefore biased at a high negative voltage, *VOP*, Figure 3. The deep n-well cathode is connected to a positive power supply, *SPAD_AVDD*, via a quench resistor.

The key is to ensure that the excess bias voltage across the SPAD when in an armed state is equal to 3.3V (for a 0.35μm process). The excess bias voltage is defined as:

$$Ve = VOP + SPAD\_AVDD - Vbd \tag{1}$$

Where Ve is the SPAD excess bias voltage, and Vbd is the reverse bias breakdown voltage of the diode. When a SPAD breaks down the reverse bias voltage across the SPAD is lowered by the quenching circuit until this voltage is brought below *Vbd*. According to Equation 1 the transition required to bring the SPAD out of avalanche breakdown is equal to *Ve*. This transition is seen at the *Vout* node in Figure 3. Being equal to 3.3V, this transition voltage can then be detected and processed by standard CMOS logic circuitry.

If the reverse bias across the SPAD is insufficient the SPAD will never breakdown. Conversely, if the reverse bias voltage is too high the SPAD will be in permanent breakdown. For the SPAD used in this project the minimum reverse bias voltage was found to be approximately 20.8V. The SPAD went into permanent breakdown at voltages above approximately 24.05V.

Dark counts are non-photon induced breakdown events and are a function of detector area and temperature. The primary causes of dark counts are thermal or tunnel generated carriers in the diode p-n junction [14]. As such, the dark count rate (DCR) of a SPAD is strongly temperature dependent. Dark count is dependent on the reverse bias voltage placed across the SPAD. As this voltage is increased, the SPADs sensitivity increases, due to the higher electric field at the p-n junction increasing the likelihood of an avalanche breakdown event. However, the increased probability of breakdown also increases the probability of a non-photon induced breakdown occurring. It is this method of electron-hole pair generation that will be used as the noise source.

After-pulsing is defined as spurious counts caused by carriers temporarily trapped in the depletion region during a breakdown event. After a short while these charges are released, causing a secondary Geiger pulse. The level of after-pulsing in a device is dependent on the quality of the silicon (which defines the trap concentration) and the number of carriers generated during a breakdown event [15]. The number of carriers generated is dependent on the parasitic

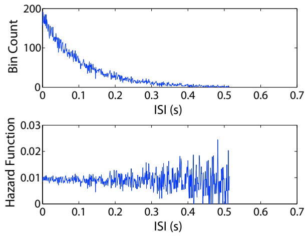


Fig. 4. The inter-spike interval (ISI) in one ms bins and hazard function of recorded dark count events from a single SPAD

capacitance of the diode and the quench circuitry used. If the hold-off time of the quench circuit is not long enough, trapped charges do not dissipate and after-pulsing occurs. As quench time increases, the correlation between the initial pulse and after-pulses decreases. After-pulsing also shows an inverse temperature dependence, increasing as temperature decreases [16].

III. Noise Recordings

The first test undertaken was to look at the events recorded from a single SPAD and plot the ISI distribution and hazard function in order to verify that the dark events being recorded from the SPADs were indeed Poisson distributed. The recorded events were first pre-processed to remove the spikes caused by after pulsing. Any spike that occurred within 100μs of the previous event was deleted from the spike train. Figure 4 shows the results and a comparison with Figure 1 confirms that a SPAD can indeed produce a Poisson distributed spike train.

The mean frequency of the spike train can be altered from 0 - 40Hz by varying VOP - the large negative voltage applied to the SPAD. This provides a good range of frequencies for neural work.

It was also important to determine that the Poisson distributed spike trains from neighbouring SPADs are independent. To test that the spike trains were not correlating, further analysis was performed on data recorded from 4 neighbouring SPADs. Each train was individually preprocessed to remove the effects of after pulsing, and the correlation between spike trains was calculated using a window size of 50ms and a bin size of 100us. If two spikes on different trains are within 50ms of each other, the time difference is recorded and binned. Figure 5 shows the cross correlations between all 4 recorded SPADs. It can be seen that no correlations are present as there are no sharp peaks in the bin count. Experiments on artificially correlated data show that even a 1% correlation is clearly visible as shown in the top right of the figure.

IV. A SPAD pixel for neural application

After verifying that SPADs located close to each other on chip produce uncorrelated spike trains, the design of an array of 1024 SPADs with Address Event Representation (AER) read-out circuitry was undertaken. The AER implementation used was Arbitrated Word Parallel AER. When a spike fires an internal request is raised, after the arbiter acknowledges it, the address of the event is placed on the address bus and the chip request signal is raised. When the receiving device has latched the address, it raises the acknowledge signal. This causes the request to be lowered, which signals the receiver to lower the acknowledge.

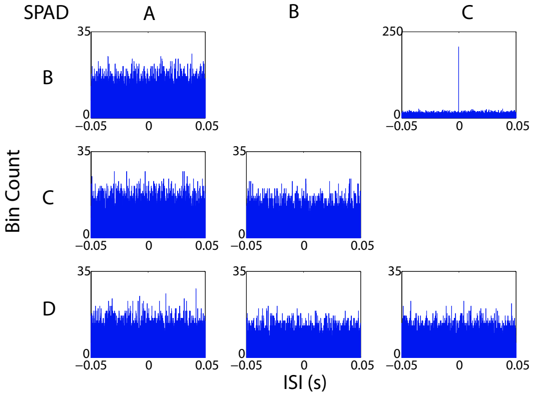


Fig. 5. The correlation between the spike trains from 4 SPADs. The trace in the top right is between two spike trains with a 1% correlation artifiically created between them. Note the prominant peak in the bin count and the change in y-axis.

Each pixel element, shown in Figure 6, contains a SPAD, a quench resistor, circuitry to interface with the AER architecture and some control logic. The control logic can restrict access to the AER bus completely or set a minimum time between requests.

The PMOS transistor (P1) acts as the quench resistor. If the gate terminal is at 0V then each avalanche event will cause a 3.3V drop on the output. The D-Type flip-flop allows each individual SPAD to be turned off. If Q is high VA is held low and Ve, the excess bias across the SPAD, is no longer enough to cause breakdown. The *SPAD_Off* signal is shifted on to the array serially in batches of 32 bits, 1 for each row. While this is happening *Program* is held high to avoid glitches on the *Spike* output.

As mentioned in section II, SPADs can exhibit after-pulsing. As this is an undesirable effect and can destroy the Poisson distributed spike train coming from the SPAD, a circuit implementing a refractory period was added. This circuitry consists of a delay cell and a current starved buffer. It produces a wider, delayed version of *Spike*. This circuit can also be used to implement a refractory period on a neural time scale so that the spike train will better mimic the statistics of a real neuron.

When *Spike* fires, the AER circuitry is activated. The SR latch output goes low, and the Active low Y request, $\overline{Ry}$, signal is pulled low. When the Acknowledge signal Ay is received $\overline{Rx}$ is also pulled low. This activates the chip request line. When an acknowledge is received from off chip, the X acknowledgment signal is asserted and the latch is set high. This deactivates the request.

This circuitry is currently being fabricated using the AMS 0.35μm High Voltage process. The chip will allow us to verify that large arrays of SPADs do not correlate and will provide

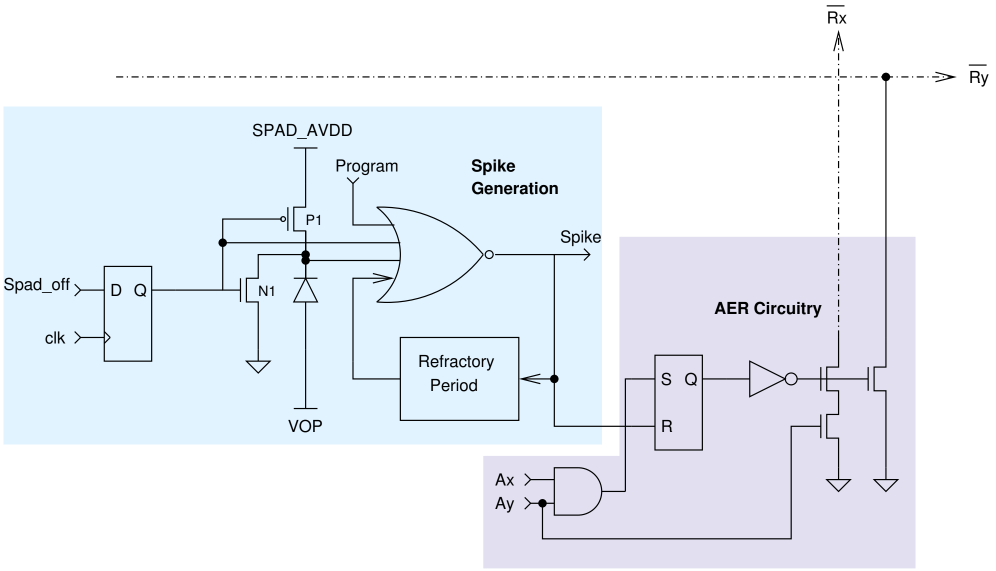


Fig. 6. The SPAD pixel including AER interface circuitry, quench resistance (transistor P1) and control logic.

genuinely random spike trains with an interface that will allow it to be integrated with other neuromorphic chips.

V. Conclusion

This paper presents data recorded from Single Photon Avalanche Diodes (SPADs) that shows that they have the potential to provide Poisson distributed spike trains suitable for neuromorphic applications. The design of circuitry that allows the removal of after pulsing and the interfacing with an AER bus is also shown. The circuitry will make possible the production of truly random spike trains that can interface to any neuromorphic chip that uses an AER read-in mechanism.

Further work is being undertaken to establish if the SPAD structure can be altered to allow control over the probability of spiking events without varying *VOP*. While the primary function of this chip is to create noise it will still function as a photon detector. The AER circuitry will also be tested to see if it can cope with the event readout under low level light conditions.

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