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A low-noise single-photon detector implemented in a 130 nm CMOS imaging process

Marek Gersbach [a,d,*], Justin Richardson [b,c], Eric Mazaleyrat [e], Stephane Hardillier [e], Cristiano Niclass [a], Robert Henderson [b], Lindsay Grant [c], Edoardo Charbon [a,d]

[a] School of Engineering, Ecole Polytechnique Fédérale de Lausanne (EPFL), CH-1015 Lausanne, Switzerland
[b] The School of Engineering, The University of Edinburgh, The King's Buildings, Mayfield Road, Edinburgh, EH9 3JL, UK
[c] STMicroelectronics Imaging Division, 33 Pinkhill, Edinburgh, EH12 7BF, UK
[d] EEMCS Faculty, Delft University of Technology, Mekelweg 4, 2628CD Delft, Netherlands
[e] STMicroelectronics, Technology R&D, Crolles, France

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ABSTRACT

We report on a new single-photon avalanche diode (SPAD) fabricated in a 130 nm CMOS imaging process. A novel circular structure combining shallow trench isolation (STI) and a passivation implant creates an effective guard ring against premature edge breakdown. Thanks to this guard ring, unprecedented levels of miniaturization may be achieved at no cost of added noise, decreased sensitivity, or timing resolution. The detector, integrated along with quenching and readout electronics, was fully characterized. A second batch of detectors with decreased n-well doping was fabricated, thus reducing the dark count rate (DCR) by several orders of magnitude. To the best of our knowledge, the DCR per unit area achieved in these devices is the lowest ever reported in deep sub-micron CMOS SPADs. Optical measurements show the effectiveness of the guard ring and the high degree of electric field planarity across the sensitive region of the detector. With a photon detection probability (PDP) of up to 36% and a timing jitter of 125 ps at full-width-half-maximum, this SPAD is well-suited for applications such as 3D imaging, fluorescence lifetime imaging, and biophotonics.

1. Introduction

Single-photon detectors such as SPADs [1] have been known for decades and have established themselves amongst the detectors of choice in several time-correlated imaging methods, such as fluorescence lifetime imaging [2–4], machine vision, and 3D imaging [5,6]. SPADs have the advantage of combining single-photon sensitivity, low noise, and timing capabilities, thus allowing to determine photon arrival times with an accuracy of only a few tens of picoseconds [5–7]. Because of these features, SPADs have been used as stand-alone detectors for a long time [8]. SPADs were first implemented in a conventional CMOS process in 2003 [9], thus allowing the integration of more and more complex electronics on the same substrate as the detector.

The integration of electronics opened the way to the fabrication of SPAD arrays, which was investigated by several groups in different CMOS technologies [10,11] as well as in custom technologies [12,13]. Generally, the functionality of these arrays is limited by the amount of electronics that can be integrated on chip; the chip size is limited by the reduction of pixel pitch that, in turn, is bounded by the scalability potential of the detector. In addition, to reach picosecond time resolutions it is generally necessary to perform time discrimination off chip. With thousands or millions of single-photon detectors, the bottleneck becomes readout, unless timing electronics is integrated on chip. One solution to cope with these constraints is to design SPADs in advanced CMOS processes with deep-submicron transistor feature size. Until now however, the use of deep-submicron process resulted in very high levels of noise in SPADs, as higher doping levels increase the intrinsic noise level of the diode. Moreover, the presence of STI and of reduced annealing steps has been shown to have detrimental effects to noise performance due to additional defects introduced in the lattice [14,15].

The SPAD structure presented in this paper addresses both miniaturization and noise concerns, proposing the use of a guard ring that comprises STI and a passivation implant. Through optical measurements, we show the effectiveness of the guard ring against premature edge breakdown, as it reduces the electric field at the edge of the device. The new n-well doping on the other hand dramatically reduces DCR, reaching levels comparable to SPADs fabricated in less advanced CMOS processes. The effects of this modification to timing jitter, PDP, and afterpulsing are negligible.

* Corresponding author. Address: School of Engineering, Ecole Polytechnique Fédérale de Lausanne (EPFL), CH-1015 Lausanne, Switzerland.
E-mail address: marek.gersbach@epfl.ch (M. Gersbach).

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The device is currently being tested in a number of applications, including time-correlated imaging, fluorescence lifetime imaging microscopy (FLIM), fluorescence correlation spectroscopy (FCS), etc.

2. SPAD implementation

The novel SPAD structure presented in this paper was implemented in a dedicated 130 nm imaging CMOS process [16]. The core of the SPAD consists of a planar p–n junction biased above breakdown, thus operating in Geiger mode. In this regime of operation, free carriers, such as photogenerated electron-hole pairs, can trigger an avalanche breakdown by impact ionization. While conventional avalanche photodiodes operate just below the breakdown voltage, where a significant optical gain can be achieved, the optical gain of a SPAD is virtually infinite, thus allowing single-photon sensitivity. This is due to the fact that a large avalanche current is allowed to flow through the diode each time a photon is absorbed in the active region of the detector. The use of a standard CMOS process allows for straightforward conversion of such an avalanche breakdown event into a digital pulse. Avalanche quenching schemes, both active and passive, are also easily integrated in these devices by means of miniaturized circuitries.

The use of a diode in Geiger mode calls for specific design techniques to avoid breakdown at its borders triggered by free carriers located at the periphery of the optically sensitive region. To avoid premature edge breakdown, a guard ring has been implemented limiting the electric field at the edges of the junction. As a result, minority free carriers located at the border of the diode will be captured by the electric field within the guard ring and cannot trigger an avalanche breakdown. This is the case as the electric field is not sufficient to sustain impact ionization. Due to its geometry, the use of STI as a guard ring yields a significant improvement in fill-factor [17]. It is however well-known that STI dramatically increases the density of deep-level carrier generation centers at its interface [14]. Thus, if the active region of the SPAD is in direct contact with the STI, as in [17], the injection of free carriers into the sensitive region of the detector results in a very high dark count rate.

In this paper we propose a technique to reduce DCR in STI-bound SPADs, while maintaining the high-density promise of STI-based implementations. In our approach, the STI region is surrounded by several passivation implants, thus creating a glove-like *p*-type structure that surrounds the STI. At the STI interface the doping level is high, which results in a very short mean free path of the minority carriers. This has the effect of drastically reducing the probability of these carriers entering the active region of the SPAD. With increasing distance from the STI, the *p*-type doping concentration is reduced in order to minimize the electric field between the guard ring and the n-well, thus reducing the probability of edge breakdown. With a properly designed guard ring the main DCR contribution in SPADs arises either from thermally generated free carriers entering the depletion region of the diode or from tunneling induced avalanche breakdown. In deep-submicron processes such as the 130 nm CMOS process used here, the wells are heavily doped and therefore tunneling is generally considered to be the dominant noise source.

To further decrease DCR we have reduced the n-well doping of the SPADs such as to diminish tunneling-induced breakdown events. After TCAD simulation four different n-well doping concentrations were implemented for this structure (only three proved to be functional).

Because of design constraints, apart from [18], only octagonal SPADs have been designed in deep-submicron technologies so far [17,19,20]. At the edges of such octagonal structures the electric field is significantly higher than in the rest of the multiplication region, thus creating regions of high noise contribution. To ensure a uniform electric field distribution across the entire p–n junction, a circular geometry was implemented in the SPAD presented here. The availability of a buried *n*-type implant allows for an ohmic contact to the n-well to be made. A schematic representation of the SPAD can be seen in Fig. 1 and a photomicrograph of the detector with integrated electronics is shown in Fig. 2.

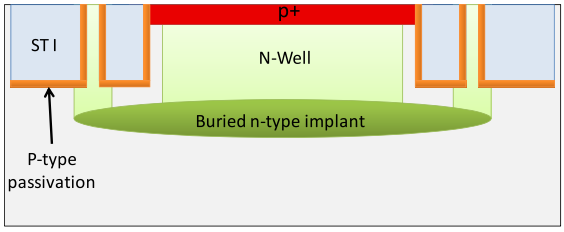

Fig. 1. Cross-section of the circular STI-bound SPAD (not to scale). The STI-interface is passivated using multiple p-type implants, thus reducing the probability of minority carriers entering the multiplication region and triggering dark counts.

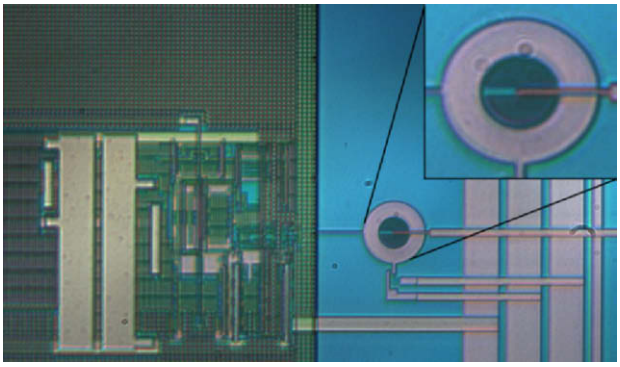

Fig. 2. Photomicrograph of the SPAD and the integrated test electronics implemented in 130 nm CMOS technology.

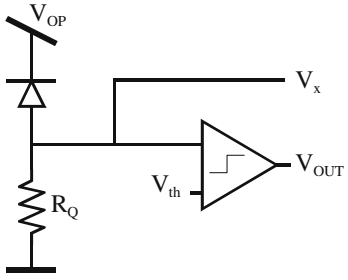

Fig. 3. Schematic diagram of the SPAD and testing electronics. The passive quenching circuit was designed as a ballast resistor. Recharge is achieved passively through the same component. Threshold detection and impedance conversion is implemented via a fast comparator.

The SPAD presented here has been integrated along with an on-chip ballast resistor and a comparator. The ballast resistance R_Q in Fig. 3 is used to perform passive quenching and recharge of the diode when operating in Geiger mode. Voltage VOP satisfies the equation

$$\mathrm{VOP} = V_E + |-V_{BD}|,$$

where V_E is the excess bias voltage and V_{BD} is the breakdown voltage. When an avalanche breakdown is triggered, the avalanche current flowing through the ballast resistance decreases the voltage across the diode. When this voltage reaches a voltage near the breakdown voltage, the avalanche current is no longer sustained

and it is quenched. The SPAD is then passively recharged by a small current flowing through the ballast resistance. The comparator, with proper threshold voltage V_{th}, is used to convert the Geiger pulses into digital signals.

3. TCAD simulation

In a properly designed SPAD the electric field must be distributed so as to have a large planar region with a high electric field density and a guard ring with much lower electric field density. In this case, any free carrier entering the planar high field region will trigger an avalanche breakdown whereas free carriers in the guard ring will cross the junction without triggering an avalanche breakdown due to the lower electric field in that region. In essence, this means that at a given excess bias voltage, the planar region is biased above its breakdown voltage whereas the rest of the diode is biased below breakdown. This can be achieved by having a lesser doped guard ring, when compared to the active region. To assess the breakdown probability in the different parts of the diode a TCAD simulations were carried out. Fig. 4. shows the electric field distribution inside the SPAD for two different n-well doping concentrations. For both cases the maximum electric field is confined in the planar region of the SPAD, i.e. the guard ring is effective in lowering the field at the border of the diode thus reducing the probability of premature edge breakdown events. Furthermore the shallow high field region ensures that a significant proportion of impinging photons will be absorbed within the active region of the SPAD. At the same time a shallow junction enables a good sensitivity to blue photons, which is generally not the case for CMOS SPADs using a less advanced fabrication process.

Generally, advanced CMOS processes use very high implant doping concentrations. As was shown in [19,20], such high doping concentrations are problematic since tunneling-induced breakdown events become dominant over thermally generated free carrier generation. As a result, all SPADs presented so far in sub quarter-micron processes yielded an unsatisfactory noise performance. Using TCAD modeling, the band-to-band tunneling probability of our device was investigated for two different n-well doping concentrations. The top panel of Fig. 5. shows that with the standard 130 nm CMOS implant the probability of band-to-band tunneling is high. Therefore a high DCR is to be expected from this device. The lower panel shows the same structure with a reduced implant doping concentration. As could be expected, the reduction of doping concentration yields a significant decrease of band-to-band tunneling. For the latter device one can expect thermally generated free carriers to be the dominant noise source.

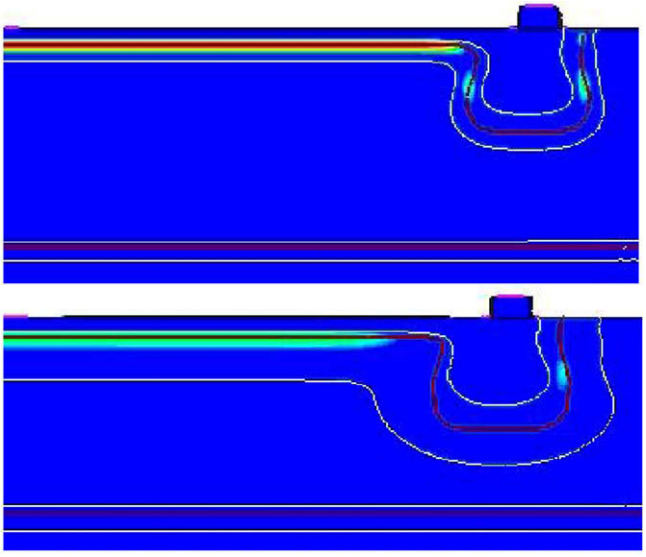

Fig. 4. TCAD simulation (arbitrary scale) of the electric field distribution in the SPAD and its guard ring. The top panel shows the electric field distribution of the SPAD with standard 130 nm CMOS implants. The lower panel shows the same structure with a n-well doping concentration reduced by a factor 5.

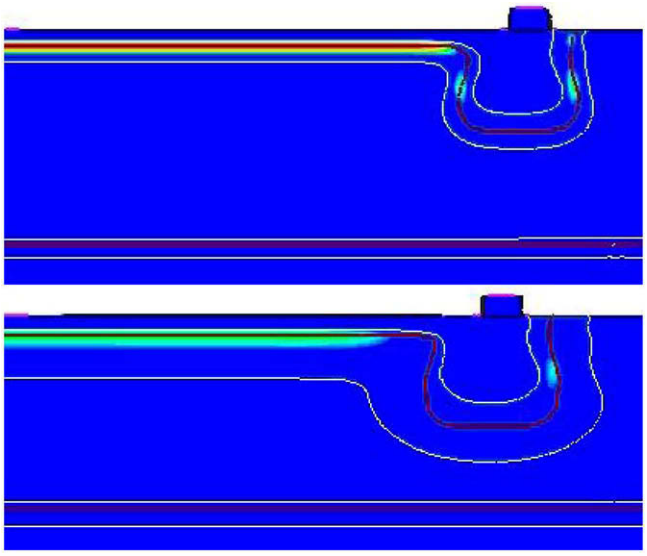

Fig. 5. TCAD simulation (arbitrary scale) of the band-to-band tunneling probability in the SPAD and its guard ring. The top panel shows the electric field distribution of the SPAD with standard 130 nm CMOS implants. The lower panel shows the same structure with a n-well doping concentration reduced by a factor 5.

4. Characterization

A p–n junction must exhibit two main characteristics in order to operate well in Geiger mode: it must show a low dark current and an abrupt breakdown behavior. In Geiger mode any free carrier crossing the high field region of the SPAD may trigger an avalanche breakdown. Thus, a low dark current proves that only few carriers are crossing the diode and are susceptible of triggering an avalanche breakdown. However, the dark current does not necessarily relate one-to-one to the DCR as the dark current may very well flow through the guard ring, where an avalanche breakdown cannot be triggered. The *I–V* characteristic was measured statically using a standard semiconductor analyzer. Fig. 6 shows the *I–V* characteristics of three diodes with the same layout but with three different n-well doping concentrations. For the SPAD with the standard doping concentration, the dark current is 5×10^{-10} A at the breakdown voltage of 9.4 V. Because of the lower doping concentration the two other devices with reduced doping show a higher breakdown voltage of 12.8 V and 17.2 V, respectively. In the interest of clarity, the rest of this article will focus on the SPAD with standard doping and the best performing device with a breakdown of 12.8 V.

When compared to older technologies, the use of advanced CMOS technologies implies higher doping levels as well as reduced annealing and drive-in diffusion steps. These factors contribute heavily to the noise floor measured in deep-submicron SPADs. For the structure presented here, even though a more advanced CMOS process was used, the novel guard ring structure and the implementation of round SPADs allowed for a drastic reduction of DCR from approximately 1 MHz in [17] to about 90 kHz (for the SPAD with standard doping) at room temperature and 1 V of excess bias, while increasing the active area of the SPAD. While the DCR is similar to the device in [19], the STI-based guard ring

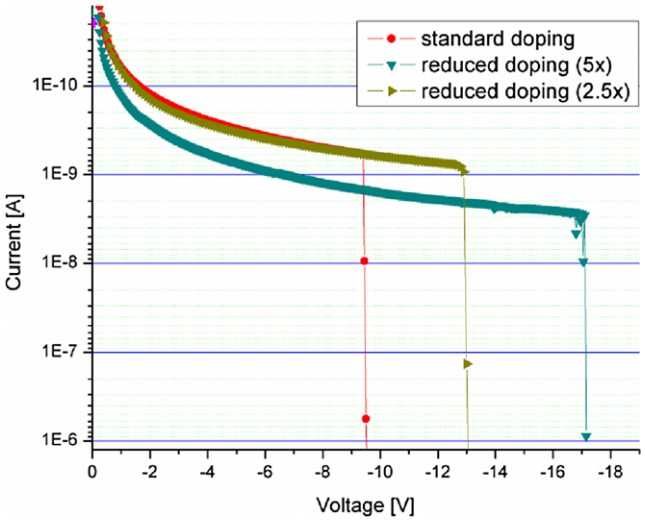

Fig. 6. *I–V* Characteristic of the SPADs with standard doping as well as with 2.5 and 5 time lower n-well doping.

structure allows for a significant improvement in fill-factor as shown in [17]. However, because of tunneling, DCR remains relatively high and the device is not suited for ultra-low light applications such as, for example, fluorescence lifetime imaging. The reduction of n-well doping allows to drastically lower tunneling probability and thus significantly decreases DCR from 90 kHz to a few 10 Hz for 1 V of excess bias. The top panel of Fig. 7. shows the temperature dependence of DCR for a SPAD with standard implants; the slope indicates that, due to the high doping levels, tunneling-induced dark counts are the dominating noise source over trap-assisted thermal generation. The lower panel shows the same measurement for a SPAD with reduced n-well doping for five different excess bias voltages. The sudden increase of DCR at temperatures exceeding 40 °C suggests that thermally generated free

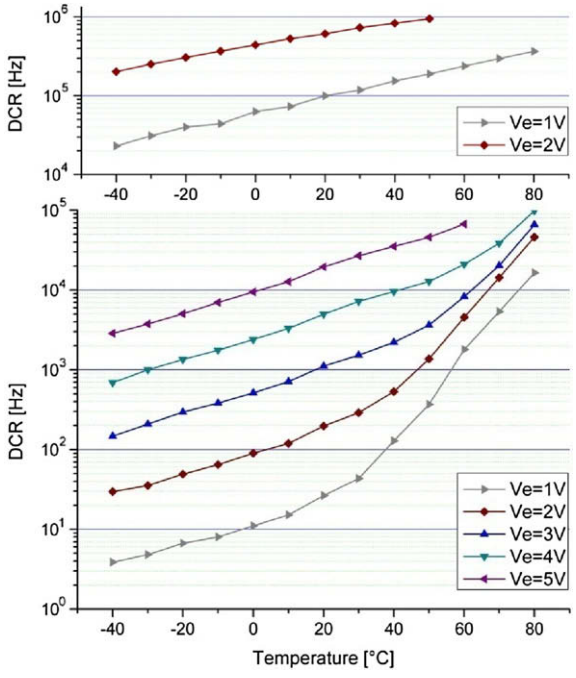

Fig. 7. Dark count rate of the SPAD as a function of temperature at 1 V of excess bias voltage for standard doping (top panel) and reduced n-well doping device (bottom panel). The slope of the curve indicates that tunneling is the dominant noise source.

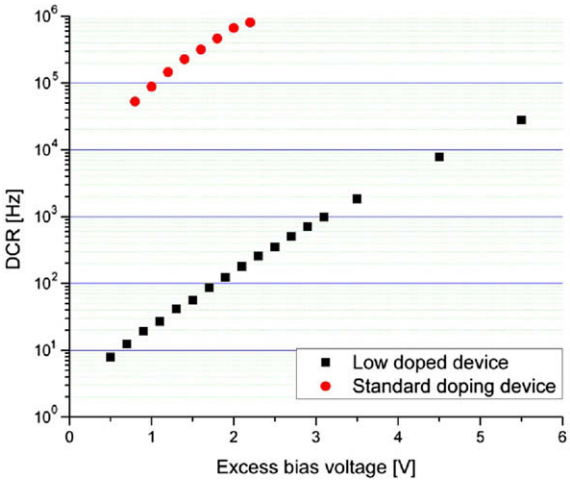

Fig. 8. Dark count rate at room temperature as a function of the excess bias voltage.

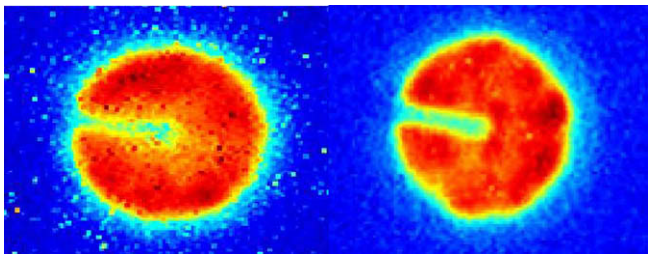

Fig. 9. Measurement of the photoemission intensity (arbitrary scale) across the SPAD during avalanche breakdown. Uniform emission indicates equal probability of breakdown on the active area. Left panel: SPAD with reduced n-well doping. Right panel: SPAD with standard doping.

carriers are the main contributors to DCR at high temperatures while tunneling dominates at lower temperatures. Fig. 8 shows the dark count rate at room temperature as a function of the excess bias voltage.

To prove the effectiveness of the guard ring and the homogeneity of the electric field across the active region of our device, an optical measurement of the photons emitted during avalanche breakdown was undertaken. The emission of photons during avalanche breakdown is directly proportional to the current intensity and thus to the electric field. During a period of 16 s a continuous avalanche current, limited to 100 μA, was allowed to flow through the diode and photoemission was captured using a microscope and a standard CCD camera.

The photoemission shown in Fig. 9 indicates that the electric field is distributed homogeneously across the sensitive region of the SPAD. Furthermore, the absence of significant emission peaks at the border of the active region shows that the guard ring is effective in lowering the electric field at the borders of the detector. Note that the region with low emission intensity in the center of the detector was the result of metal shielding due to the conductor connecting the center of the p^+ implant. These measurements are in good agreement with the TCAD simulations showing a homogenous electric field distribution.

The sensitivity of the SPAD over a wide spectral range has also been investigated. The use of an imaging CMOS process gave us access to an optimized optical stack and thus allowed for a good PDP. With a standard doping concentration the measured PDP peaks at 28% at 480 nm of wavelength for an excess bias voltage of 2 V. As a comparison, the SPAD fabricated in standard 0.18 μm technology in [20] achieved a maximum PDP of only 5.5% at 2 V of excess bias. Decreasing the n-well doping allows to significantly reduce DCR

and therefore permits to bias the SPAD with higher excess voltages while keeping noise at a reasonable level. The PDP of the device with reduced doping is similar to that of the standard device for the same excess biases. At 5 V of excess bias the PDP is 36% while DCR is approximately 11 kHz. As most deep-submicron processes, the 130 nm CMOS process used here has very shallow implants and thus the sensitive region of the SPAD is located very close to the silicon surface. As a result, the PDP is improved for shorter wavelengths and the maximum PDP is found at only 480 nm of wavelength. The measurements were obtained using a standard monochromator system coupled to an integrating sphere (LOT Oriel Group Europa) and a calibration detector (Hamatsu). Note that for each PDP measurement the mean DCR was subtracted from the measured count rate, thus DCR is not responsible for an artificially increased PDP.

Another important measurement for time-correlated applications is the time response of the detector. To assess its time-resolution, the SPAD was illuminated by a picosecond laser diode source emitting 40 ps pulses at 40 MHz repetition rate and with 637 nm of wavelength (Advanced Laser Diode Systems GmBH, Berlin, Germany). The time interval between the laser output trigger and the leading edge of the SPAD signal was measured using the time-to-digital converter embedded in a high performance oscilloscope (LeCroy 8600A). By repeating this measurement a sufficient amount of times, a histogram of photon arrival times can be created. At 1 V of excess bias voltage, the timing jitter of the entire system (including laser, detector and TDC jitter), at full-width-half-

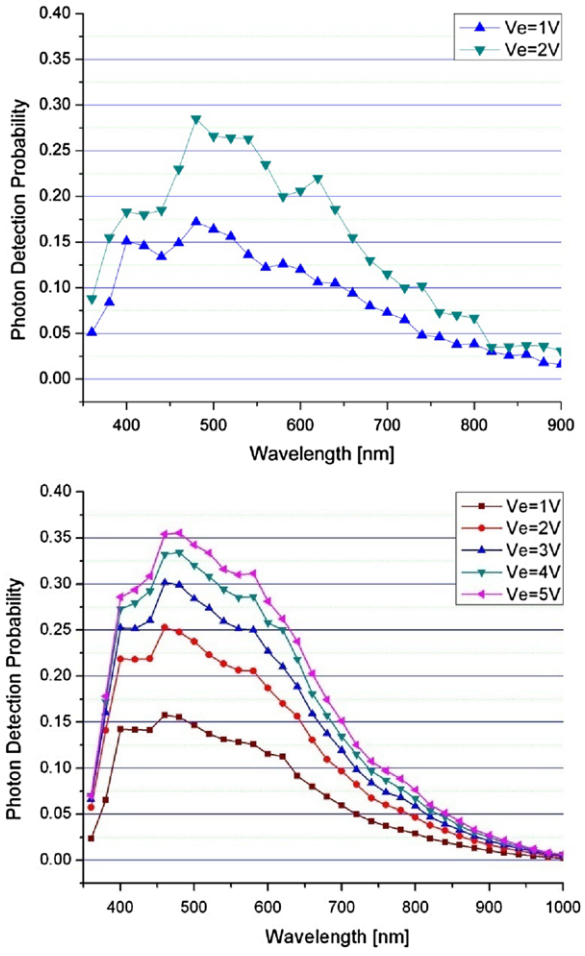

Fig. 10. Photon detection probability. The top panel shows the photon detection probability at one and two volts of excess bias for the SPAD using the standard implant; the bottom panel shows the photon detection probability for excess bias voltages ranging from one to five volts.

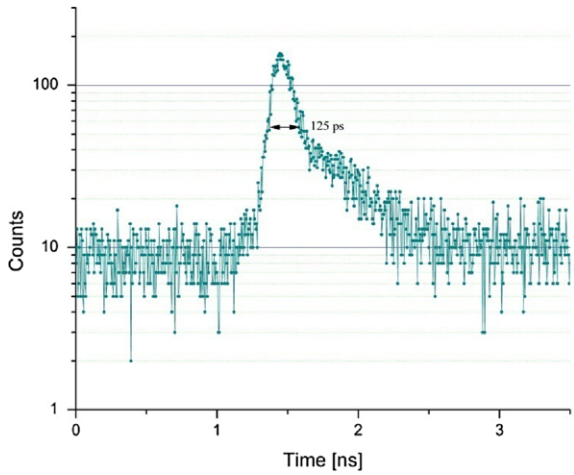

Fig. 11. Time response of the SPAD when illuminated by a picosecond light source at 637 nm wavelength and 1 V of excess bias voltage.

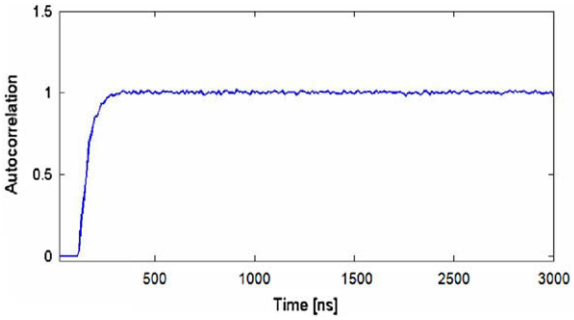

Fig. 12. Autocorrelation probability of the SPAD. No afterpulsing contribution could be measured.

maximum was measured to be 125 ps. As can be seen from the right-hand side of the measured time response in Fig. 9, the absorption of photons underneath the active region of the SPAD creates a tail in the time response as the generated free carriers diffuse back into the multiplication region (Fig. 10).

During an avalanche breakdown event, a significant amount of charge carriers flows through the diode. Some of these carriers may be trapped in the multiplication region of the diode and subsequently released, thus triggering a second avalanche breakdown. This process is known as afterpulsing. To limit the probability of afterpulses, it is necessary to limit the amount of charges flowing through the diode during an avalanche breakdown event; this can be done by limiting the capacitance at the borders of the diode. In our case, the use of a CMOS process enables on-chip integration of the quenching resistance and of the readout electronics in the immediate surroundings of the detector, thus limiting parasitic capacitances (Fig. 11).

A reduced parasitic capacitance at the avalanching node has beneficial effects on afterpulsing as it reduces the overall carriers involved in an avalanche and thus the probability that a secondary avalanche is triggered.

To assess the afterpulsing probability, the correlation between subsequent breakdown events was measured. Fig. 12 shows the autocorrelation curve we obtained. Note that after each breakdown event the SPAD needs to recharge and is thus inactive for a certain amount time, known as dead time. For the structure presented here the dead time is approximately 180 ns. Therefore, in the first 180 ns after a breakdown event, the autocorrelation is zero. When the SPAD is fully recharged the autocorrelation is stable around one, proving that no afterpulsing events are present. Since the les-

Table 1
Performance summary at room temperature.

Performance	Standard SPAD		Low-doped SPAD		Unit
	Typ.	Max.	Typ.	Max.	
PDP @ Ve = 2 V		30		26	%
PDP @ Ve = 5 V		n.a.		36	%
DCR @ Ve = 2 V	670		0.22		kHz
DCR @ Ve = 5 V	n.a.		11		kHz
Active area	58		58		μm^2
FWHM time jitter @ Ve = 1 V	125		128		ps
Afterpulsing probability	<1		n.a.		%
Dead time	180		n.a.		ns
Breakdown voltage	9.4		12.8		V

ser doped SPAD was not integrated with a read-out buffer its afterpulsing probability could not be measured. However, it is expected that the afterpulsing performance will not be deteriorated by the reduction of n-well doping.

The performance of the detector presented in this paper is summarized in Table 1.

5. Conclusion

The SPAD presented in this paper combines the advantages of deep-submicron processes, such as the possibility of integrating complex electronics and improved fill-factor thank to a STI-based guard ring. As a result, the noise performance was improved by more than an order of magnitude, when compared to other STI-bound SPADs. Furthermore the reduction of n-well doping decreased the DCR by an additional three orders of magnitude.

The first integration of SPADs along with quenching and read-out electronics in 130 nm CMOS technology presented here also enabled us to show the absence of afterpulsing for a detector dead time of 180 ns. Finally, optical measurements of the photoemission during avalanche breakdown proved the effectiveness of the guard ring structure and the planarity of the multiplication region. We thus believe that the structure presented here is well-suited for the fabrication of large detector arrays which can be used in low-light time-correlated single-photon applications such as fluorescence lifetime imaging or 3D imaging.

6. Disclaimer

This publication reflects only the authors' views. The European Community is not liable for any use that may be made of the information contained herein.

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References

[1] Cova S, Longoni A, Andreoni A, Cubeddu R. A semiconductor detector for measuring ultraweak fluorescence decays with 70 ps FWHM resolution. IEEE J Quantum Electron 1983;10(4):630–4.
[2] Gersbach M, Boiko DL, Sergio M, Niclass C, Petersen C, Charbon E. Time-correlated two-photon fluorescence imaging with arrays of solid-state single photon detectors. In: Conference on lasers ans electro-optics Europe (CLEO Europe); 2007.
[3] Mosconi D, Stoppa D, Pancheri L, Gonzo L, Simoni A. Single-photon avalanche diode CMOS sensor for time-resolved fluorescence measurements. In: Proc ESSCIRC; 2006. p. 564–7.
[4] Rae BR, Griffin C, Muir KR, Girkin JM, Gu E, Renshaw DR et al. A microsystem for time-resolved fluorescence analysis using CMOS single-photon Avalanche diodes and micro-LEDs. In: Proc ISSCC; 2008. p. 44–5.
[5] Niclass C, Rochas A, Besse PA, Charbon E. Design and characterization of a CMOS 3-D image sensor based on single photon Avalanche diodes. IEEE J Solid State Circ 2005;40(9):1847–54.
[6] Stoppa D, Pancheri L, Scandiuzzio M, Gonzo L, Dalla Betta G-F, Simoni A. A CMOS 3-D imager based on single photon Avalanche diode. IEEE Trans Circ Syst I 2007;54(1).
[7] Zappa F, Tisa S, Gulinatti A, Gallivanoni A, Cova S. Monolithic CMOS detector module for photon counting and picosecond timing. In: Proc ESSDERC; 2004. p. 341–4.
[8] Cova S, Ghioni M, Zappa F, Rech I, Gulinatti A. A view on progress of silicon single photon Avalanche diodes. Adv Photon Count Tech Proc SPIE 2006;6372:63720I–1.
[9] Rochas A, Gani M, Furrer B, Besse PA, Popovic RS, Ribordy G, Gisin N. Single photon detector fabricated in a complementary metal–oxide–semiconductor high-voltage technology. Rev Sci Instrum 2003;74(7):3263–70.
[10] Niclass C, Rochas A, Besse PA, Charbon E. Towards a 3D camera based on single photon Avalanche diodes. IEEE J Sel Top Quantum Electron 2004;10(4):796–802.
[11] Niclass C, Favi C, Kluter T, Gersbach M, Charbon E. A 128 × 128 single-photon imager will on-chip column-level 10b time-to-digital converter array capable of 97 ps resolution. In: Proc ISSCC; 2008. p. 44–5.
[12] Tudisco S, Musumeci F, Lanzanò L, Scordino A, Privitera S, Campisi A, Cosentino L, Condorelli G, Finocchiaro P, Fallica G, Lombardo S, Mazzillo M, Sanfilippo D, Sciacca E. A new generation of SPAD-single photon Avalanche diodes. IEEE Sensor J 2008:8.
[13] Zappa Franco, Gulinatti Angelo, Maccagnani Piera, Tisa Simone, Cova Sergio. SPADA: single-photon Avalanche diode arrays. IEEE Photon Technol Lett 2005:17.
[14] Mamamoto T. Sidewall damage in a silicon substrate caused by trench etching. Appl Phys Lett 1991;58(25):2942–4.
[15] Kwon HI, Kang MI, Park B-G, Lee JD, Park SS. The analysis of dark signals in the CMOS APS imagers from the characterization of test structures. IEEE Trans Electron Dev 2004;51(2):178–84.
[16] Cohen M, Roy F, Herault D, Cazaux Y, Gandolfi A, Reynard JP, Cowache C, Bruno E, Girault T, Vaillant J, Barbier F, Sanchez Y, Hotellier N, LeBorgne O, Augier C, Inard A, Jagueneau T, Zinck C, Michailos J, Mazaleyrat E. Fully optimized Cu based process with dedicated cavity etch for 1.75 μm and 1.45 μm pixel pitch CMOS image sensors. IEDM 2006.
[17] Finkelstein H, Hsu MJ, Esener SC. STI-bounded single-photon Avalanche diode in a deep-submicrometer CMOS technology. IEEE Electron Dev Lett 2006;27(11):887–9.
[18] Marwick MA, Andreou AG. Single photon avalanche photodetector with integrated quenching fabricated in TSMC 0.18 μm CMOS process. Electron Lett 2008;44(10).
[19] Niclass C, Gersbach M, Henderson R, Grant L, Charbon E. A single photon Avalanche diode implementation in 130-nm CMOS technology. IEEE J Sel Top Quantum Electron 2007;13:863–9.
[20] Faramarzpour N, Deen MJ, Shirani S, Fang Q. Fully integrated single photon Avalanche diode detector in standard CMOS 0.18-μm technology. IEEE Trans Electron Dev 2008;55(3):760–7.