2.2 A Gamma, X-ray and High Energy Proton Radiation-Tolerant CIS for Space Applications

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Photon counting is useful in space-based imagers wherever quantitative light-intensity evaluation is necessary. Various types of radiation, from cosmic rays to high-energy proton beams to gamma radiation, have an effect on the functionality and accuracy of imagers and the literature is extensive [1,2]. Techniques to maximize sensor tolerance have also been developed for a number of years and several imagers resistant to up to 30Mrad (Si) of gamma radiation have been reported. These sensors have several shortcomings: either significant noise performance degradation, up to several orders of magnitude [2], or unacceptably high pre-radiation noise levels [3]. In addition, many radiation-tolerant sensors use dedicated processes, thus possibly limiting their suitability for mass-market applications [4].

In this paper we describe a CMOS photon-counting imager designed to detect the Earth's airglow, which is the atmospheric oxygen emission at 762nm due to oxygen recombination. Airglow occurs day and night and enables geostationary and orbiting satellites to infer their position referred to the Earth's center for attitude determination [5]. The goal is to develop a sensor that reduces the requirements on weight and size of navigational telescope optics mounted on an ultra-low-cost micro-satellite.

Figure 2.2.1 shows the imager concept and examples of airglow emission under distinct conditions. The sensor, operating in photon-counting mode, consists of an array of 32×32 pixels. Each pixel comprises a single-photon detector, a 1b counter and fast readout circuitry. Radiation hardness is achieved with a combination of schematic and physical design techniques, while keeping pixel complexity to a minimum and spreading all its components uniformly. This is done to minimize the probability that radiation particles damage a vital section of the chip. Contrary to the general trend in the literature, the fill factor is kept low. This has the advantage of reducing the probability that the detector is hit by radiation, while light is reclaimed using optical concentrators, currently being fitted onto the array. Finally, due to the digital nature of the detector, a higher resilience to charge injection due to irradiation is built into the sensor.

A block diagram is shown in Fig. 2.2.2. The timing diagram of the sensor readout is shown in the inset. The array is read out in rolling-shutter mode via the high-speed row decoder, and may be reset after each read operation or read out non-destructively. The column decoder is used to issue a readout control signal while the signal conditioning synchronizes it with the clock. All 32 columns are read in parallel, thus enabling a complete 1024-pixel frame readout in T_{min}=1.2µs with 1b depth. To achieve a higher number of gray levels we accumulate N frames, thus reaching an intensity resolution of $\log_2(N)$ bits at the expense of lower frame rates. The saturation count rate is $1/T_{min}$, SNR_{max} for integration time t_{int} is computed as

$$SNR_{\max} = 20\log\left(\frac{t_{\text{int}}}{T_{\min}}\right) - 10\log\left(\frac{t_{\text{int}}}{T_{\min}} + \text{Var}[DC]\right)$$

where noise power is given by the sum of Poisson noise power and Var[DC], i.e. the variance of the stochastic process underlying dark count generation. The latter is approximated by the average of dark counts during integration, or DCR t_{int}, where DCR is the dark count rate of the detector. Median DCR is used since we believe that this figure is a better representation of the noise performance of the chip than a simple average, as it represents the DCR upper bound for 50% of the pixels.

The schematic of the pixel is shown in Fig. 2.2.3(a). The detector is implemented as a single-photon avalanche diode (SPAD), the counter as a latch, and the readout as a pull-down transistor. The SPAD is a pn junction biased above breakdown so as to operate in Geiger mode. In this design, the avalanche voltage is sensed by M2 that forces the latch to logic 1. Transistor M7 acts as pull-down of the column line that is kept high by resistor R_{PU}, while M6 is the row selection switch, controlled by RowSEL. When the column is pulled down, a buffer (not shown) controls a pad and the output of the chip for that column is interpreted as a photon detected in the previous interval of time. Transistors M4 and M5 are controlled respectively by a column line (ColSET) and row line (RowSET) to force the static memory of a specific pixel to logic 1, irrespective of the SPAD state, for testing purposes. M8 is used to operate a global or row-based reset via signal gRESET, whereas M3 prevents memory conflicts in case of a SPAD firing during reset. SPAD quenching and recharge are performed by M1 that can be adjusted globally via signal BIAS, so as to select a proper trade-off between dead time and afterpulsing probability [6]. The pixel comprises 10 NMOS and 2 PMOS transistors, thus enabling minimization of n-well surface, and ensuring a pitch of 30µm.

To sustain massive doses of radiation, measures are taken at the layout level as well. Most of the NMOS transistors are implemented in source-surrounded-by-gate style to minimize defect-induced leakage. Other radiation hardening techniques include an increase of certain design rules, extensive use of contacts to minimize potential latch-up, and the implementation of n+ and p+ trenches at well boundaries. The layout of the pixel is shown in Fig. 2.2.3(b). The SPAD is implemented as a p+/p-well/deep n-well junction, based on [6]; its cross-section is shown in Fig. 2.2.3(c). The breakdown voltage V_{BD} of the SPAD is 17.7V. At its cathode, a bias voltage of 21V is applied to operate with an excess bias voltage V_E of 3.3V. Thanks to this configuration, a lower capacitance at the sensing node is achieved, thus reducing the charge involved in an avalanche and also reducing optical crosstalk and after-pulsing at a given dead time.

Figure 2.2.7 shows a micrograph of the chip, whose total surface area is 2.00×2.35mm^2. The sensor is first tested for speed and functionality. For this test, we use a breadboard system based on a dual-FPGA board similar to [7]. In the current firmware implementation, the minimum integration time is 2.6µs, limited by a clock frequency of 48MHz. The chip is also tested for sensitivity, signal uniformity, and noise performance. The results of the full characterization of the chip are reported in the table of Fig. 2.2.6(a). The radiation testing was performed in 3 separate measurement campaigns. Gamma radiation was performed using a standard ^{60}Co source. The sensor received a total dose of 1Mrad (Si), followed by 172h of annealing at 80°C. The median DCR measured during the experiment is reported in Fig. 2.2.4(a). The statistics of the session are reported in detail in Fig. 2.2.6(b). We also exposed a sensor with identical detectors but different pixel and system electronics, not optimized for radiation hardness [7]. The sensor sustained a catastrophic failure at 2kRad and no recovery was possible after annealing.

In the second experiment, the sensor was exposed to 2 separate proton beams at a constant energy of 11MeV and 60MeV, respectively. Figure 2.2.4(b) shows the median DCR vs. dose for a maximum of 40krad. The evolution of the DCR distribution over the array for the gamma irradiations is shown in Fig. 2.2.5

In the third experiment, the chip was exposed to a massive X-ray dose. The X beam, generated by a bipolar metal-ceramic tube, achieves fluence and total dose levels reported in Fig. 2.2.6(b). The table also lists the results of the DCR change. Preliminary irradiations were performed without any filtering and using a large collimation (27 mm). A series of irradiations at 15kV, 120kV and 200kV show negligible impact on DCR, PDP, and afterpulsing.

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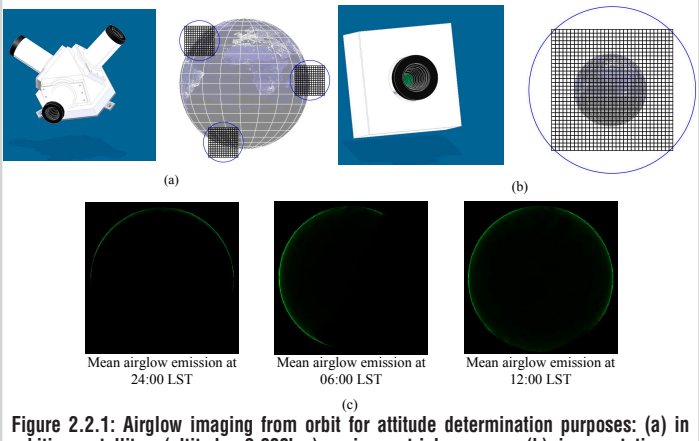

Figure 2.2.1: Airglow imaging from orbit for attitude determination purposes: (a) in orbiting satellites (altitude: 2,000km), using a triple sensor; (b) in geostationary satellites (altitude: 36,000km) using a single sensor. The grids indicate the observation window of each sensor and the lateral resolution with a FOV of 20°. (c) The center wavelength of airglow emission is 762nm with a minimum estimated photon flux of 6400counts/s/pixel [5].

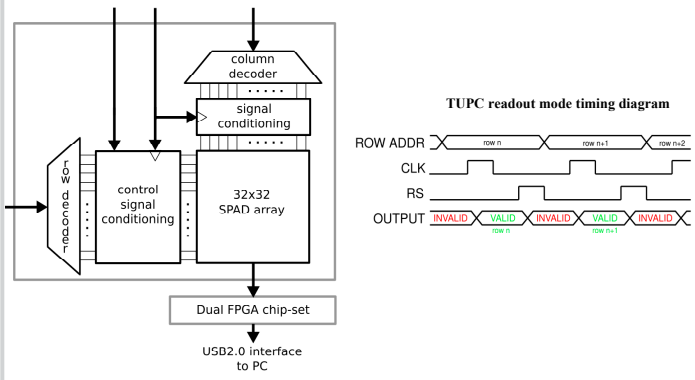

Figure 2.2.2: Block diagram of the sensor system. The inset shows the basic timing diagram for time-uncorrelated photon counting mode. Rows are read out in rolling shutter mode with or without row-wise reset (RS). CLK determines the minimum integration time.

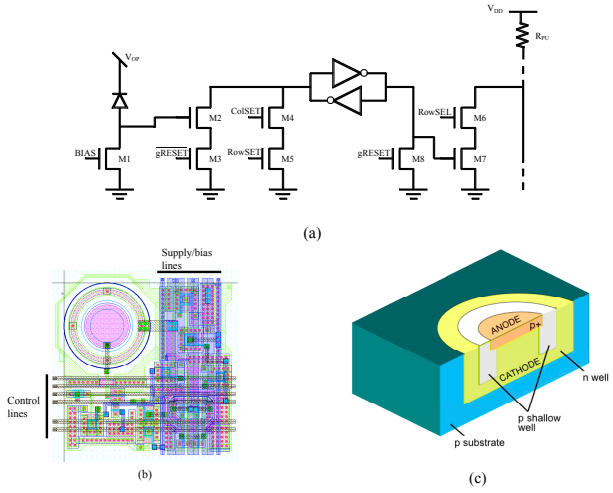

Figure 2.2.3: (a) Pixel schematic comprising a SPAD, a 1b static memory, and a pull-down mechanism for fast readout. (b) Pixel layout with most NMOS transistors implemented in source-surrounded-by-gate style. Active area minimized with heavy use of contacts to minimize the chance of latch up. (c) Cross-section of the SPAD.

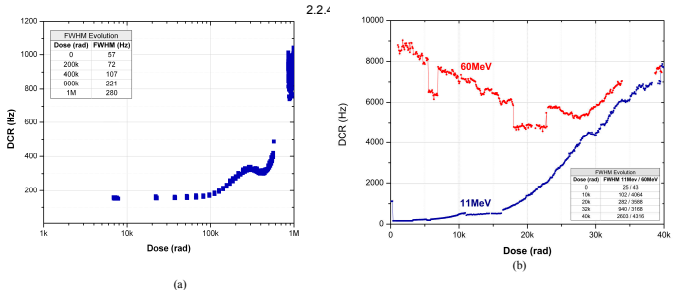

Figure 2.2.4: Median DCR evolution during 3 irradiation experiments before annealing: (a) gamma irradiation; (b) proton irradiation (11MeV; 60MeV). All measurements conducted at room temperature.

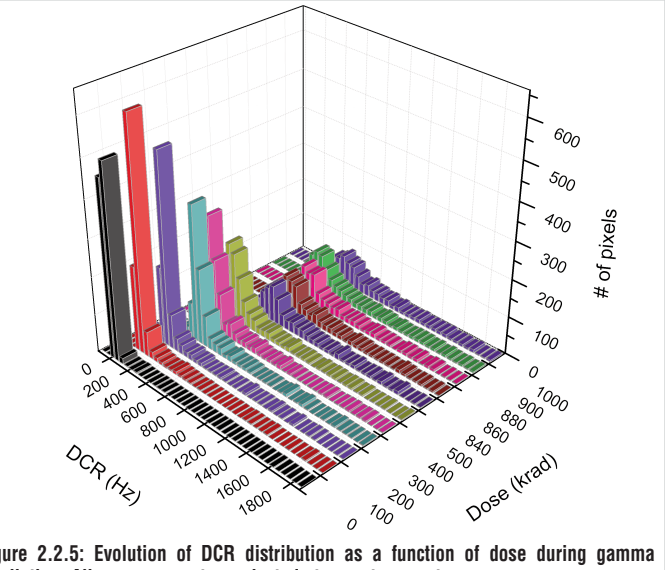

Figure 2.2.5: Evolution of DCR distribution as a function of dose during gamma irradiation. All measurements conducted at room temperature.

Parameter	Measurement	Unit	Conditions
Array size	32x32	-	
Pixel size	30x30	µm²	
Size of the active spot of a pixel	6	µm	diameter
Die size	2.0x2.35	mm²	
Minimum integration time	2.66	µs	1.2µs @ 96MHz clock frequency
Clock frequency	48	MHz	limited by firmware
Photon detection probability (PDP)	35	%	At 500 nm, V_x=3.3V
Excess bias voltage (V_x)	1~3.3	V	
Sensitivity spectrum	350-to-850	nm	> 3% PDP
Afterpulsing probability	<1	%	
Maximum frame rate	375,939	fps	1b of resolution
	1,468	fps	8b of resolution
	367	fps	10b of resolution
	12	fps	15b of resolution
Dark count rate (DCR) (median / time-varying component)	98	Hz	-40 °C, V_x=3.3V
	104		-20 °C
	129		0 °C
	140 / 9.83		+23 °C
	182		+40 °C
Dynamic range	90	dB	
Signal-to-noise ratio	45	dB	12 fps, V_x=3.3V
Signal uniformity	<1	%	
Power consumption	113.8	mW	frame rate: 375,939fps, 1b
	110.0	µW	frame rate: 367fps, 1b
Technology	0.35µm CMOS	-	

(a)

Irradiation type	Source	Fluence/ Flux	Dose (Si)	Initial DCR	Final DCR	DCR after Annealing (anneal time)
Gamma	Co60	10.46rad/min	1.0Mrad	153	1020	276 (172h)
X	Comet-Yxlon TU320-D03	4.3AsV²	0.25mGy	540	545	540 (1min)
		324AsV²	0.25mGy	540	640	540 (1min)
		900AsV²	0.5mGy	540	701	540 (1min)
Proton	Accelerator	$1.8x10^9$p/cm²/s (11MeV)	40.0krad	140	6298	3884 (10d)
		$8.3x10^8$p/cm²/s (60MeV)	40.0krad	142	6290	1299 (21d)

(b)

Figure 2.2.6: (a) Performance summary for the image sensor. (b) Irradiation experiment summary. DCR is reported in Hz at room temperature. PDP, afterpulsing probability, and maximum frame rate remain unchanged after all three types of irradiation.

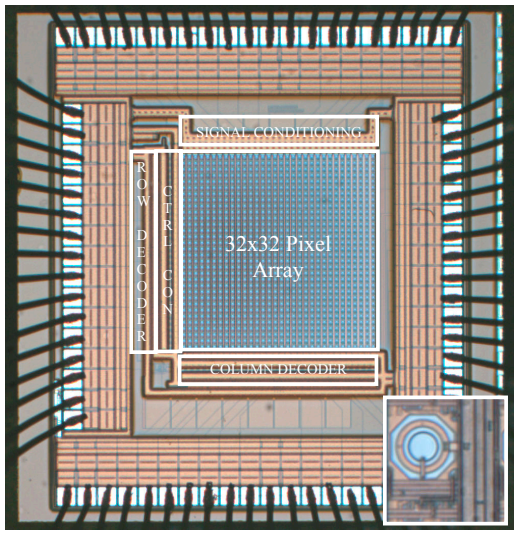

Figure 2.2.7: Die micrograph of the 0.35µm CMOS sensor chip. The circuit has a surface area of 2.0×2.35mm^2. The pixel (inset) has a pitch of 30µm.

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