A 32x32-Pixel Array with In-Pixel Photon Counting and Arrival Time Measurement in the Analog Domain

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***Abstract*— A Time-to-Amplitude Converter (TAC) with embedded analog-to-digital conversion is implemented in a 130-nm CMOS imaging technology. The proposed module is conceived for Single-Photon Avalanche Diode imagers and can operate both as a TAC or as an analog counter, thus allowing both time-correlated or time-uncorrelated imaging operation. A single-ramp, 8-bit ADC with two memory banks to allow high-speed, time-interleaved operation is also included within each module. A 32x32-TACs array has been fabricated with a 50-µm pitch in order prove the highly parallel operation and to test uniformity and power consumption issues. The measured time resolution (LSB) is of 160 ps on a 20-ns time range with a uniformity across the array within ±2LSBs, while DNL and INL are 0.7LSB and 1.9LSB respectively. The average power consumption is below 300µW/pixel when running at 500k measurements per second.**

I. INTRODUCTION

Today the cost of solid-state two-dimensional imagers has dramatically dropped, introducing low cost systems on the market suitable for a variety of applications, including both industrial and consumer products. However, these systems can capture only a two-dimensional projection (2D), or intensity map, of the scene under observation, losing a variable of paramount importance, i.e., the arrival time of the impinging photons. Time-resolved imaging systems offer great potential of improvement in many areas such as machine vision, where they are used to extract the distance information of the objects in the scene [1], or in life sciences where investigation tools such as fluorescence-lifetime imaging microscopy (FLIM) allow the mapping of many cell parameters and the detection of pathologies or DNA sequencing [2]. To measure the arrival-time of impinging photons a TDC or TAC is needed. However, these devices are typically based on complex circuits [3]-[6], whose area occupation and power consumption makes their integration impossible at a pixel level. Many efforts have been recently done in the integration of time-measurement circuits, both TDC and TAC, together with Single-Photon Avalanche Diode (SPAD). In [7] 32 TDCs have been implemented on chip serving an array of 128x128 SPAD based pixels, while [8] reports an example of in-pixel implementation, in a linear array, of a TAC. The recent possibility to fabricate SPADs in deep-submicron CMOS technologies, as proven in [9]-[10], makes it now possible to integrate TAC/TDC within each pixel, allowing fully parallel operation as required when operating at very high frame rate.

In this paper we propose a circuit, fabricated in a 130-nm imaging CMOS technology, capable of operating both as a TAC or as an Analog Event Counter (AEC), making it suitable for both time-correlated or time-uncorrelated imaging. The TAC/AEC circuit implements an embedded 8-bit A/D conversion and allows a time-interleaved operation up to 500 kframes/sec. The proposed module has been successfully integrated with a SPAD (fully described in [9]) in a 50-µm pixel, and arranged in an array of 32x32-pixels. The design and characterization of the developed TAC/AEC circuit is here reported.

II. TAC/AEC ARCHITECTURE

The block diagram of the proposed pixel is sketched in Figure 1. It consists of a SPAD, with relative quenching circuitry, an analog stage, which can operate both as TAC or AEC, a digital control logic aimed at driving the TAC/AEC block, a time-interleaved, single-ramp ADC and two 8-bits memory benches. This architecture allows two different sensing modes: in time-uncorrelated mode the pixel will detect and count the number of photons within a given observation time-window, while in the time-correlated mode the time interval between the photon arrival time and a reference clock (STOP)

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is measured. Since these data are not required simultaneously, the AEC and the TAC have been realized by sharing, as far as possible, the same analog circuitry in order to reduce the pixel area.

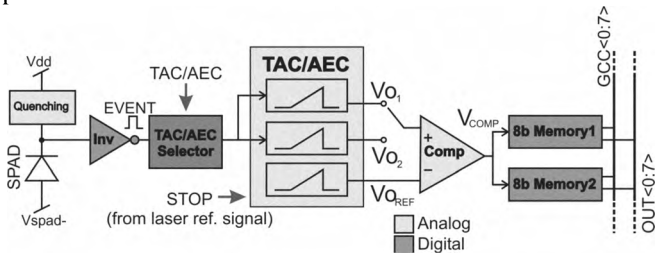

Figure 1. Pixel block diagram.

The digital pulse generated by the SPAD/Inv ensemble is first processed by the TAC/AEC digital selector stage which generates either a fixed time-width pulse (AEC-mode) or a pulse (TAC-mode) whose time-width is proportional to the time occurred between the rising edge of the event signal (EVENT) and the falling edge of the clocking signal STOP. This digital pulse drives the analog TAC/AEC stage depicted in Figure 2.

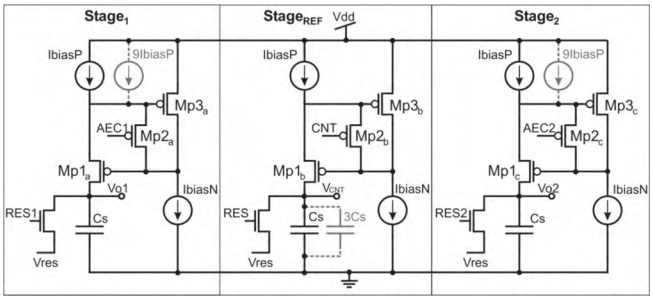

Figure 2. Circuit schematic of the TAC/AEC stage.

The basic cell consists of a current source (*IbiasP*) which charges up capacitor *Cs* when the switch-structure, composed by M_{p1},M_{p2},M_{p3} and *IbiasN*, is turned on. This architecture used for the switch implementation allows achieving higher linearity, faster time response, and lower charge injection effect with respect to the conventional single switch or current steering approaches [6],[8].

The basic building block used to generate the voltage ramp is replicated into three layout-matched structures: $Stage_1$ and $Stage_2$ are used alternatively to measure the number of events or the event arrival time in a time interleaved way, while $Stage_{REF}$ is used to generate a reference voltage ramp used to implement the embedded ADC. In the following the two operation modes are detailed:

A. Time-uncorrelated Mode (AEC)

When working as AEC, each detected photon activates the charge of capacitors *Cs* for a fixed time slot T_{Ck}, thus producing a voltage step $\Delta V = IbiasP \cdot T_{Ck} \cdot 1/C_s$ at nodes $Vo_{1,2}$.

In this mode the TAC/AEC selector is used to generate, starting from the global reference clock signal STOP, the control signals AEC1,2, so that a very precise control on T_{Ck} is achieved. In order to capture intensity images at 500 kframe/s an upper limit of 2µs for the observation and A/D conversion windows has been considered. At the end of the observation window capacitor *Cs* contains the analog information proportional to the number of counted photons. At this point, the reference TAC/AEC block is externally stimulated by the signal CNT (globally distributed to the whole pixel matrix, synchronously with the 6-bit Gray Code Counter GCC), while the output of AEC/TAC selector is applied to the second AEC branch (time interleaved operation) and Vo_1 is connected to the comparator. As the number of CNT pulses increases, the voltage at node Vo_{CNT} increases and when it reaches the same voltage previously stored on Vo_1 the voltage comparator toggles thus sampling the digital code GCC<0:5> into the memory (only 6 bits are possible at full operation speed of the AEC).

B. Time-correlated Mode (TAC):

In this mode only the arrival time of the first detected photon within the observation window (2µs) is measured.

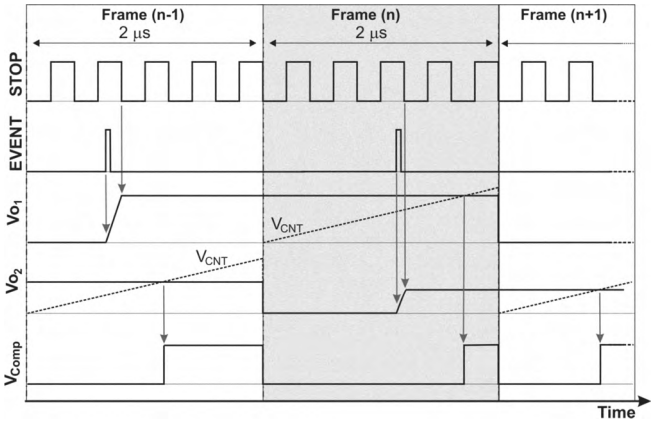

Figure 3. Simplified timing diagram of the TAC operation mode.

As illustrated in Figure 3, the voltage ramp is started each time a photon is detected, while the charge up of capacitors *Cs,* within $Stage_{1,2}$, is stopped by the system clock (to map a 25-ns time range a 40-MHz frequency is used for the STOP signal). Differently from the AEC, during the analog-to-digital conversion phase it is not possible to stimulate the reference block at the same speed of the TAC (the voltage ramp is now generated within a few nanoseconds). To cope with this problem, the voltage ramp is properly scaled in this modality, by increasing to $4 \cdot Cs$ the integrating capacitor of $Stage_{REF,}$ and setting to $10 \cdot IbiasP$ the current sources of $Stage_{1,2}$. The ratio of 40 achieved in this way allows the mapping of very short time intervals using affordable frequencies for the digital coding signals GCC<0:7>.

A 3.3V power supply has been used for all the analog circuitries, while deep-sub micron transistors, powered at 1.2V, have been used for the digital part. This choice guarantees that the output voltage swing of the analog stage is maximised, thus improving the SNR. A voltage translator has been used to interface the digital part to the analog one. The

resulting layout of the pixel, with the main blocks evidenced is shown in Figure 4.

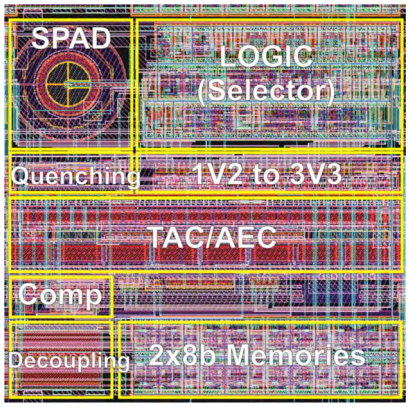

Figure 4. Layout of the designed 50-µm pixel.

III. Chip Architecture

The 32x32-pixel array has been integrated together with programming registers, a PLL (used to generate the reference clock starting from a low frequency input signal), reference voltage generators (band-gap), row and column decoders and column read out circuitries (see Figure 5).

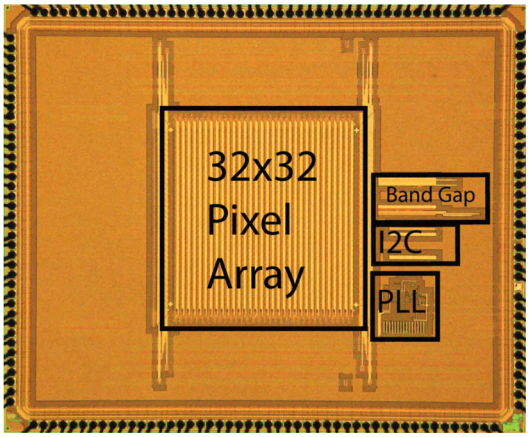

Figure 5. Chip photo-micrograph, with the main functional blocks highlighted.

The array is split into two 32x16 sub-arrays which are read out in parallel, with a row wise pixel address, by column serializers placed at the top and bottom of the array and buffered out by 2x32 I/O pads, achieving a maximum output data-rate of more than 4 Gbit/s. Clock-tree structures have been used to distribute the reference clock and high-speed signals to each rows, while extensive use of decoupling capacitors and dedicated power-grid for the pixel power supply allow reducing ground bounce effects.

IV. Experimental Results

The sensor has been fabricated in a 130-nm imaging CMOS technology and the chip, housed in a 180 pin CPGA, fully characterized. Unfortunately, due to a conflict in the data-bus access by the pixel, only 7-bits (out of 8-bits) can be read-out.

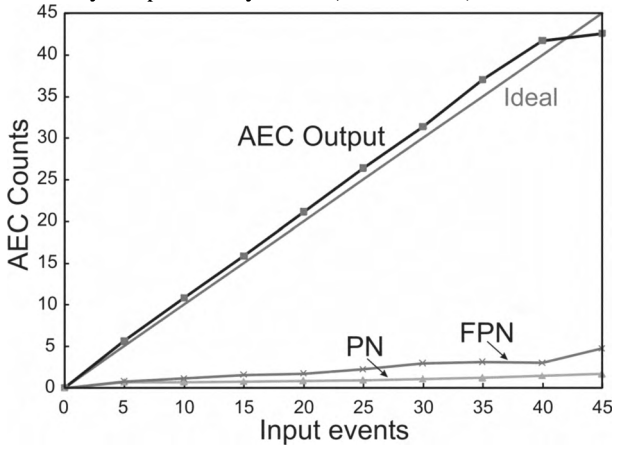

Figure 6. AEC measured input/output characteristics, with relative PN and FPN, at 500 kframes/sec. Input events are referred to a 2µs time-window.

This is not affecting the AEC performance, where 6-bits were expected, but limits to 7-bits the TAC resolution. The AECs performance was tested applying a digital stimulus, simulating the SPAD activity, to all the pixels. The digitized AEC output, in response to the input clock, is shown in Figure 6 exhibiting a good linearity and resolution up to 40 counts, which corresponds to a 20-MHz count frequency.

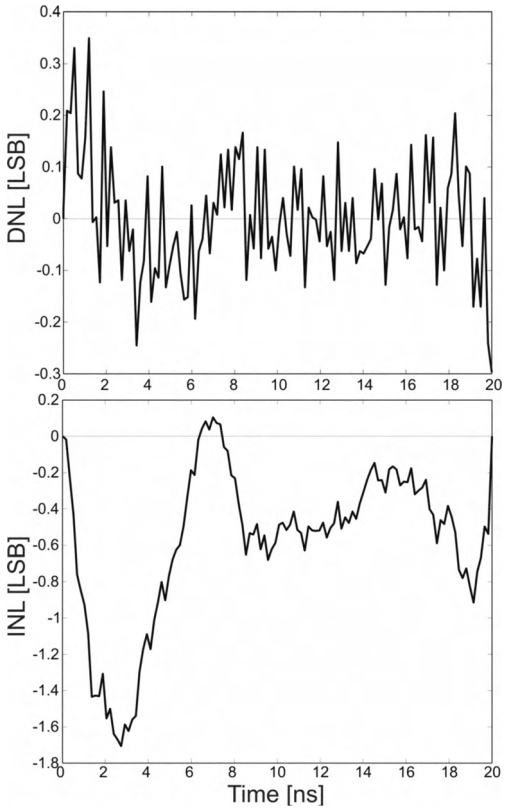

Figure 7. Measured TAC DNL and INL on a 20-ns time range (LSB =160 ps).

Fixed-Pattern-Noise and Pixel-Noise, extracted on the whole pixel-array, are less than 3LSB and 1.3LSB respectively. When the input stimulus has a frequency too close to the global clock STOP, distortion phenomena appear because the TAC/AEC Selector starts missing events. However, the maximum number of counts achieved corresponds to the upper-limit of the SPAD dead-time (50-ns).

Code Density Test [11] has been used to extract the INL and DNL figures of the TAC. As can be seen from Figure 7, INL/DNL values are 1.9LSB/0.7LSB respectively over a 20-ns time range. By changing the sensor settings also different time-ranges can be mapped.

Jitter noise and TACs uniformity have been extracted by applying a digital stimulus, generated by means of an external FPGA, to the whole pixel array, spanning the whole 20-ns time-range and acquiring thousands of frames to obtain a significant statistical population.

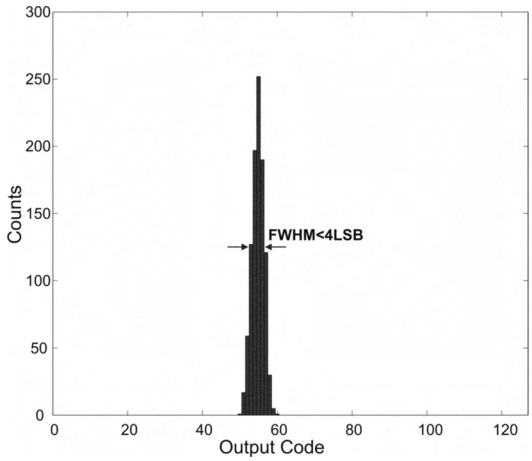

Figure 8. Measured TAC jitter noise in response to an electrical stimulus having a constant time-delay.

The worst-case FWHM of the counts histogram produced by the TAC-array in response to a input signal, having a constant phase-shift with respect to the clock signal STOP, is shown in Figure 8.

TABLE I. SUMMARY OF THE CHIP PERFORMANCE.

	PARAMETER	VALUE	NOTE
TAC	Time range	20 ns	Adjustable
	Bit resolution	7 bits	8 bits expected
	Time resolution (LSB)	160 ps	-
	Uniformity	±2 LSB	-
	INL	1.9 LSB	-
	DNL	0.7 LSB	-
	Time Jitter	< 600 ps	@ FWHM
AEC	Bit resolution	6 bits	
	Max count frequency	20 MHz	
	FPN, PN	3 LSB, 1.3 LSB	
	Area	< 1300 μm^2	-
	Pixel power consumption	200 µW (Analog) 100 µW (Digital)	@ 500kframe/s

LSB, Uniformity, INL, DNL are extracted considering a 20-ns time range.

This noise figure is comprehensive of the FPGA jitter noise contribution and can be considered as a worst case estimation of the TAC noise on the whole time-range.

The main characteristics of the proposed work are summarized in Table 1.

V. CONCLUSIONS

In this paper a 32x32-pixel array, with in-pixel photon counting and photon arrival-time measurement capability, has been fabricated and tested. The proposed TAC/AEC architecture with embedded ADC makes the structure immune to process variation effects, obtaining excellent uniformity along the array and a very compact layout.

The highly parallel sensor architecture, combined with the time-interleaved operation and in-pixel A/D conversion, allows for a throughput data rate exceeding 4 Gbit/s, making this sensor suitable for high-speed imaging applications, where both intensity and time-resolved measurements are required.

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