A 128 × 128 Single-Photon Image Sensor With Column-Level 10-Bit Time-to-Digital Converter Array

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***Abstract*—An imager for time-resolved optical sensing was fabricated in CMOS technology. The sensor comprises an array of 128 × 128 single-photon pixels, a bank of 32 time-to-digital-converters, and a 7.68 Gbps readout system. Thanks to the outstanding timing precision of single-photon avalanche diodes and the optimized measurement circuitry, a typical resolution of 97 ps was achieved within a range of 100 ns. To the best of our knowledge, this imager is the first fully integrated system for photon time-of-arrival evaluation. Applications include 3-D imaging, optical rangefinding, fast fluorescence lifetime imaging, imaging of extremely fast phenomena, and, more generally, imaging based on time-correlated single photon counting. When operated as an optical rangefinder, this design has enabled us to reconstruct 3-D scenes with milimetric precisions in extremely low signal exposure. A laser source was used to illuminate the scene up to 3.75 m with an average power of 1 mW, a field-of-view of 5° and under 150 lux of constant background light. Accurate distance measurements were repeatedly achieved based on a short integration time of 50 ms even when signal photon count rates as low as a few hundred photons per second were available.**

***Index Terms*—Depth sensor, FCS, flash laser camera, fluorescence lifetime imaging microscopy (FLIM), Förster Resonance Energy Transfer (FRET), Geiger-mode avalanche photodiode, rangefinder, range imaging, single-photon avalanche diode, single-photon detector, solid-state 3-D imaging, SPAD, TCSPC, time-correlated single-photon counting, time-of-flight, 3-D image sensor.**

I. Introduction

In a conventional camera, a scene is projected onto the image plane, where a multipixel sensor captures its intensity. In a time-correlated or time-resolved camera, each pixel evaluates the phase or time-of-arrival (TOA) of impinging photons, in addition to light intensity. Time-resolved optical imaging has many uses in disciplines such as physics, molecular biology, medical sciences, and computer vision, just to name a few. In particular, deep subnanosecond timing resolution, in combination with high sensitivity, is becoming increasingly important in a number of imaging methods.

Time-resolved optical sensing may be accomplished using a conventional camera by optical means, such as stroboscopic illumination or fast optical shutters [1]. However, these methods are limited in the achievable time resolution. Streak cameras are a good alternative, however high costs often prevent their use in many applications. For picosecond time resolution, the sensors of choice are today single-photon counters that, in a variety of solid-state and nonsolid-state incarnations, have existed for decades. The two most successful single-photon counters to date are microchannel plates (MCPs) and photomultiplier tubes (PMTs). While PMTs are generally used as a single pixel single-photon detector and do not allow imaging without scanning, MCPs have demonstrated such capability. However, MCPs require high bias voltages and ultralow pressure to operate. In addition, cost and size have limited their use to low-scale and scientific applications [2].

As an alternative to MCPs and PMTs, researchers are increasingly turning to avalanche photodiodes (APDs). Even though they have been known for several decades, APDs have been proposed for time-resolved sensing relatively recently. Besides being solid-state devices, APDs can be advantageously operated in Geiger mode when biased above breakdown. In this mode of operation they are known as single-photon avalanche diodes (SPADs). SPADs can reliably detect single photons and their TOA precisely. The timing properties of SPADs have been studied extensively [3]. However, only recently researchers have shown that SPADs may be built in CMOS technologies [4]. The research activity that has followed has been aimed at showing scalability of SPADs in a variety of technologies [5]–[7]. With demonstration of large arrays of SPADs [8], [9], number and diversity of applications of SPAD arrays have multiplied.

Time-resolved imaging has been one of the first target applications of SPAD arrays. Time-resolved imagers can be employed to characterize the relaxation of specific molecules from an excited to a ground state, for example, by measuring the lifetime of photon emitted by the molecule. Specific applications in this domain range from fluorescence-based imaging, such as Förster resonance energy transfer (FRET), fluorescence lifetime imaging microscopy (FLIM) [10], and fluorescence correlation spectroscopy (FCS) [11]. Other techniques used in biology and physics can also take advantage of time-resolved imaging. Such techniques are, for example, voltage sensitive dye (VSD) based imaging [12], [13], particle image velocimetry (PIV) [14], instantaneous gas imaging [15], etc.

Another very important application of SPAD arrays relates to multipixel rangefinding and 3-D imaging. The literature of rangefinders based on conventional detectors is extensive and two methods are generally preferred for the measurement of time-of-flight (TOF). The first measures TOF using modulated illumination and a modified CCD [16], [17]. A precise charge

Manuscript received April 28, 2008; revised July 17, 2008. Current version published December 10, 2008. This work was supported by a grant of the Swiss National Science Foundation.

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Digital Object Identifier 10.1109/JSSC.2008.2006445

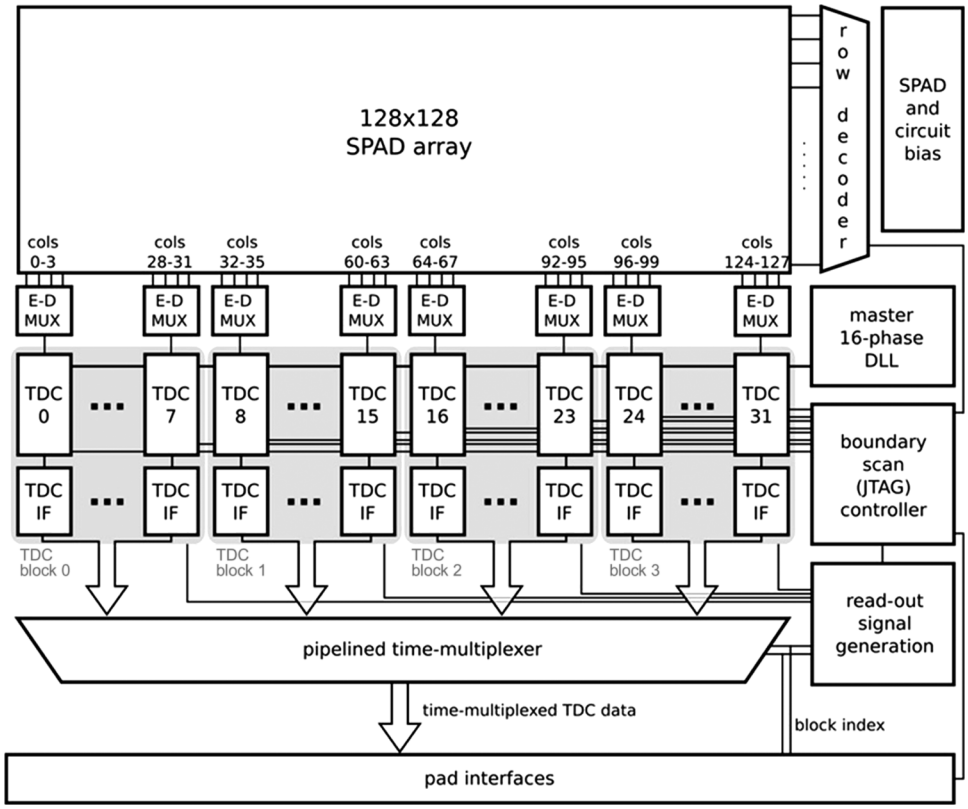

Fig. 1. Block diagram of the proposed sensor. The sensor consists of a 128 × 128 pixel array, a bank of 32 TDCs, and a fast parallel readout circuitry. A row decoding logic selects 128 pixels that are activated for detection. The pixels are organized in groups of four that access the same TDC based on a first-in-take-all sharing scheme.

transfer technique is used to evaluate the phase difference in-pixel. The phase difference appears as a small voltage that is integrated over many measurement cycles to improve accuracy. One of the most important challenges of this method is the suppression of noise (both optical and electrical) and of background illumination. This problem is often addressed by implementing symmetric pixels where the phase accumulates as a differential mode voltage while the noise sources are a common mode signal that can easily removed. CMOS sensors have also been used to implement modulation based TOF methods. In [18] and [19] for example charge transfer and quantum efficiency modulation schemes were used to achieve the same functionality as in their CCD homologues. In [1] on the contrary, low-cost high-speed electronic shuttering in the optical path is used in combination with a conventional CMOS camera.

The second method is based on a direct measurement of TOF using a pulsed illumination source. In these devices, the delay is often computed by means of a time-to-amplitude-converter (TAC) placed in the pixel and driven by the pixel's detector [20]–[22]. To reach subnanosecond resolution, fast pixel amplifiers, in combination with high-power sources, are necessary. Due to the size of the resulting circuitry, pixels are either large and in low numbers.

SPAD rangefinders based on pulsed illumination have been proposed by several researchers using both single pixel [23] (with scanning) and multiple pixel [24]–[26] (scannerless) solutions. Our group was the first to propose a multipixel rangefinder based on CMOS SPADs [5], [27]. Others have pursued SPAD arrays in dedicated technologies [28]. With the growth of the array size however, it has become increasingly hard to process massive volumes of data from SPAD pixels. To address this issue, hybrid systems have been proposed by [29] that combine advanced CMOS technologies with processes designed to optimize SPAD performance. The approach introduced by [29] was to place front-end circuit and a high speed counter close to the detector. However, since detector and ancillary circuitry were placed in two different chips, complex and expensive 3-D integration techniques were needed to bond two incompatible technologies. In addition, the parasitics introduced by the bonding resulted in reduced performance.

In this paper we propose a monolithic approach to high-performance time-resolved imaging. The sensor was fabricated in a 0.35-μm CMOS technology and it comprises an array of 128 × 128 SPAD pixels, a bank of 32 time-to-digital converters (TDCs) for on-chip time measurements, and a high-speed data I/O. The system integration achieved in the present work is unprecedented and the resolution achieved by the proposed chip demonstrates the gains that can be made if a fully integrated approach is used.

By proper sharing of resources (in this case 32 TDCs), we demonstrated that large arrays can be achieved while keeping chip size small. Every group of 4 pixels in a row share a TDC based on an event-driven mechanism similar to [9]. As a result, row-wise parallel acquisition is obtained with a low number of TDCs. In alternative to TDCs, analog design techniques have also been used to evaluate the photon's TOA on-chip [22], [26]. However, increased pixel size and potentially complex schemes

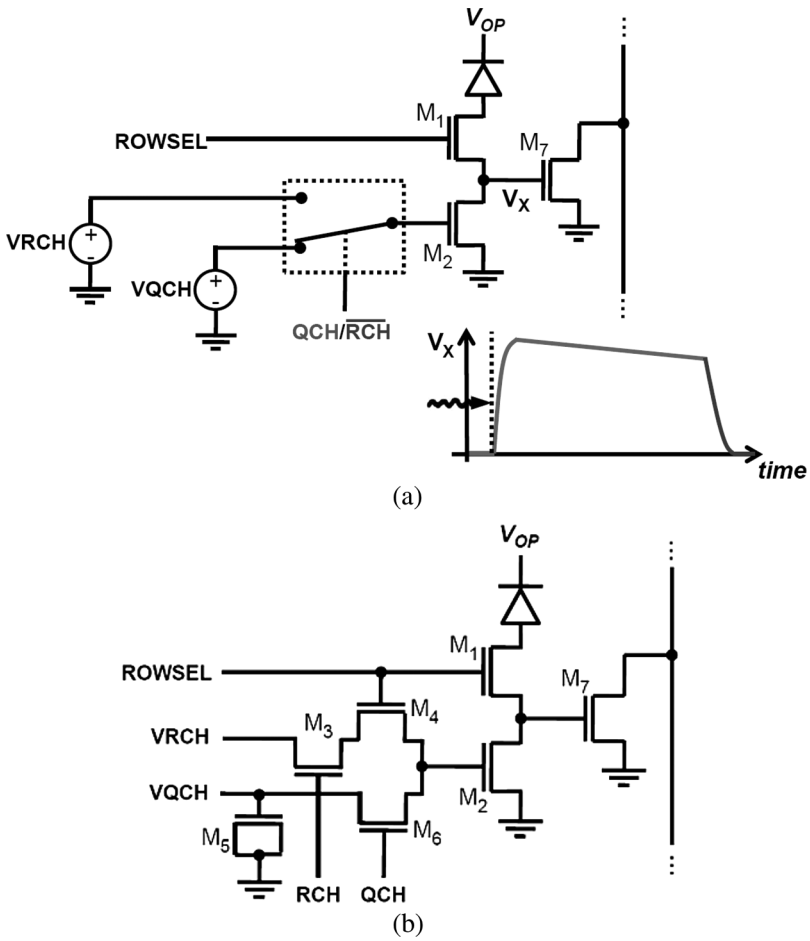

Fig. 2. (a) Principle of pixel circuit providing passive quenching and active recharge and an example of signal waveform on photon detection. (b) Schematics of actual pixel implementation.

for temperature and technological variability compensation are often needed.

II. Sensor Design

A. Imager Architecture

In Fig. 1, a block diagram of the image sensor is shown. The sensor consists of an array of 128 × 128 single-photon pixels based on a 0.35 μm SPAD design, reported in [6]. A bank of 32 TDCs was integrated on the same integrated circuit. TDCs are utilized to compute time-interval measurements between a global start signal and photon arrival times in individual pixels. A row selection decoder is used to activate one row of 128 pixels that have access to the bank of TDCs. In this design, the 32 TDCs are shared among 128 pixels in a given row. The sharing scheme is based on a 4:1 event-driven readout [9] that allows the 128 pixels in a row to operate simultaneously. Since every TDC is shared among four pixels, time-to-digital conversion time was highly optimized at design phase so as to improve throughput.

Calibration of TDCs is implemented on-chip based on a master delay-locked loop (DLL) that locks against an external reference frequency, generated by a crystal oscillator. As a result, TDC resolution and linearity is maintained over process, voltage and temperature (PVT) variations.

At the bottom of the TDC array, a high-speed digital readout circuit handles the data generated by all the TDCs. It consists of a pipelined 4:1 time-multiplexer that operates at a frequency at least four times faster than the data generated in every TDC. A readout controller generates all the signals utilized internally and implements a readout protocol interface. Most of digital building blocks in the TDC and readout circuitry provide duplicated (shadow) registers that may be read and written via an on-chip JTAG controller. The JTAG controller offered advantageous testing and characterization possibilities.

B. Pixel Circuit

Single-photon detection capability is achieved in the pixel via a p+/deep n-well SPAD, using p-well as guard-ring [6]. At room temperature, the breakdown voltage V_{BD} of the SPAD in this design is 17.7 V. At its cathode, a bias voltage (V_{OP}) of 21 V is applied in order to operate nominally with an excess bias voltage (V_E) of 3.3 V, above V_{BD}. Miniaturization constraints lead to a solution based on a NMOS-only circuit for the pixel. The SPAD front-end and readout circuit consists of 7 NMOS transistors. Fig. 2(a) shows a simplified schematic of the pixel circuit, which implements passive quenching and active recharge. A row selection transistor (M_1) decouples the SPAD anode from pixels in the rows that are not selected. At the selected row, the SPAD is charged as a result of its anode being

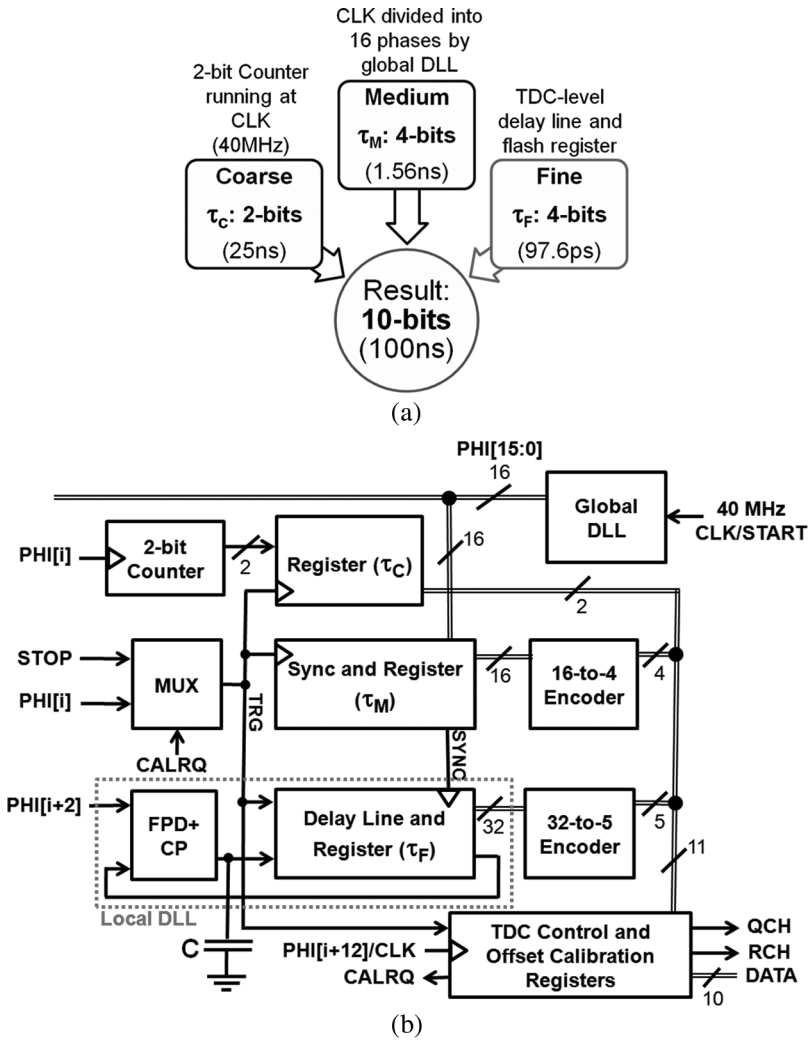

Fig. 3. (a) TDC interpolator principle. Coarse and medium resolution are generated globally and fine resolution is implemented on each TDC. This solution leads to an efficient area implementation while achieving large measurement range. (b) Simplified TDC block diagram.

connected to ground via quenching/recharge transistor M_2. Passive quenching and active recharge is controlled by means of a switch that connects the gate-to-source voltage of M_2, $V_{GS,2}$, to either $VQCH$ or $VRCH$. Prior to any photon detection, $V_{GS,2}$ is connected to $VQCH$, a low voltage, thus, providing a very high impedance from node V_X to ground. This impedance is typically higher than one megaohm. When a photon triggers the SPAD, the avalanche current induces a voltage across M_1 which pulls V_X towards V_E, according to the waveform shown at the bottom of Fig. 2(a), thus quenching the SPAD. This voltage transition, which carries the arrival time of a photon, is accurately transferred to the column line via the output transistor M_7. At the bottom of the column, the corresponding TDC starts performing a time-to-digital conversion. During the conversion time, since M_2 still provides a high impedance path to ground, the SPAD is maintained in dead-time while V_X decreases very slowly towards ground. Note that the waveform shown in Fig. 2(a) is not to scale. When the TDC is at the end of a conversion, it triggers the switch position so as to apply a recharge voltage V_{RCH} on $V_{GS,2}$, thereby performing a well-defined active recharge. From this point, the pixel is able to detect subsequent photons.

In Fig. 2(b), the actual implementation of the pixel circuit is shown. Transistors M_3, M_4, and M_6 implement the switches to set $V_{GS,2}$. M_5 is used as a capacitor to reduce the effect of switching noise on $VQCH$ caused by charge injection from the gate of M_2. Signals QCH and RCH are generated by the TDC controller. At the bottom of each column, a signal shaping circuit ensures that QCH and RCH are nonoverlapping, so as to prevent current to flow from $VRCH$ to $VQCH$. The column line potential is kept high by pull-up transistors at the bottom of the column when it is inactive. Bias voltages V_{OP}, $VQCH$, and $VRCH$ are global for the pixels in the SPAD array. In particular, $VQCH$ and $VRCH$ are distributed by means of a number of analog buffers so as to insure stable reference voltages.

C. Time-to-Digital Converter

A very critical component involved in the design of picosecond-resolution time-resolved imager is the TDC. In this work, initial requirement specifications were: a) 10-bit reso-

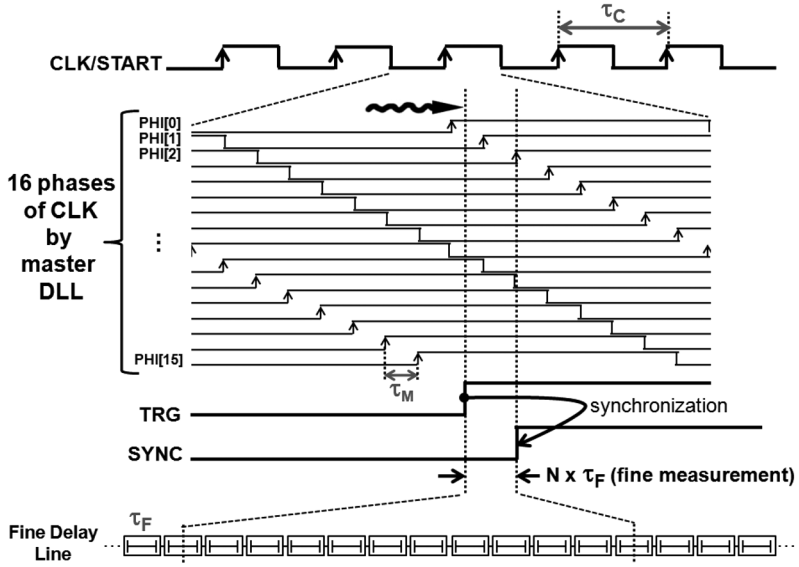

Fig. 4. Waveform of key signals involved in a TDC.

lution TDC with adjustable least significant bit (LSB) value ranging from 70 to 200 ps; b) automatic calibration against PVT variations; c) high-throughput with a maximum conversion time of 100 ns; d) suitable to be replicated several times on the same chip; and e) scalability for future deep-submicron designs.

Taking into account all these requirements, a careful solution research leads to a TDC based on a three-level interpolator. Based on this principle, the TDC combines coarse (τ_C), medium (τ_M), and fine (τ_F) resolutions to resolve a measurement range of 10 bits with a LSB value equal to τ_F. The TDC interpolation principle is schematically shown in Fig. 3(a). A global clock signal CLK modulated at a frequency of 40 MHz is used as a PVT-invariant reference signal. The period of CLK is used to set τ_C, it is then split into 16 uniformly shifted phases PHI[15:0] by means of a global DLL. The delay between two adjacent phases, i.e., between PHI[i] and $\mathrm{PHI[i+1]}$, is used as τ_M. Typically, τ_C and τ_M are 25 and 1.56 ns, respectively. At the TDC level, a very short delay of 97.6 ps is synthesized out of PHI[15:0] and used as τ_F. Finally, an appropriate interpolation based on a linear combination of τ_C, τ_M, and τ_F enables the measurement of a time interval within a typical range of 100 ns. This solution has a number of advantages. Multilevel interpolation allows for the determination of relatively long time intervals with high resolution without the need for long delay lines, while distributing relatively low frequency signals only. Long delay lines usually occupy relatively large silicon area. Moreover, when a signal propagates through a long delay line, it accumulates timing jitter, thus causing a broadening of timing uncertainty. The proposed solution is advantageous especially when a large array of TDCs ought to be implemented. Since τ_C and τ_M are synthesized globally, they do not use additional circuit area at TDC level. As a result, small and low power TDCs may be obtained.

In Fig. 3(b), a simplified block diagram of a TDC is shown. An example of the waveform of key signals involved in the time-to-digital conversion is illustrated in Fig. 4. The main TDC structure is similar to the design reported in [30]. Nonetheless, further improvements have been implemented so as to reduce the silicon area and to perform flash conversion, thus increasing throughput. Each TDC has an independent controller that is used as a time interpolator, to generate internal signals, and to control its operating mode. Each controller also manages the interface with the global readout circuit and with the column circuitry. The TDC supports two main operating modes: (i) a measurement mode and (ii) a calibration mode. In measurement mode, the STOP signal originated by the first of four SPADs that detects a photon is mapped to signal TRG in the column-level TDC via a multiplexer, i.e., signal CALRQ is deasserted. TRG precisely and securely registers the state of the 2-bit coarse counter as well as the state of 16 phases, thereby generating two and four bits of conversion data, respectively.

In order to determine the four remaining least-significant bits, i.e., fine resolution, the next transition of PHI[15:0] following the assertion of TRG is of interest. Simultaneously to registering coarse and medium resolutions, signal TRG is also fed into a 32-tap fine delay line, whose propagation state is sampled on the next transition of PHI[15:0]. This is achieved by signal SYNC, which is generated in the medium resolution register, shown in Fig. 5(a). Metastability issues make it difficult to rely on the exact first transition of PHI[15:0] to assert SYNC. Indeed, when the setup time of a register is violated, its clock to output propagation time suffers from large dispersion, thus potentially impairing the performance of the TDC. In order to prevent this issue, the circuit of Fig. 5(a) skips the right first transition and securely asserts SYNC on the second transition of PHI[15:0], thus, resulting in a timing accurate synchronization signal.

The time interval between TRG and SYNC is measured by determining how far TRG propagates in the fine delay line before SYNC is asserted. The fine delay line and associated fast register are shown in Fig. 5(b). The fine delay line consists of two chains of optimized inverters. An input STRT (TRG) signal is converted to a fully-differential signal, whose transitions are aligned via an edge aligner circuit. Each component of the dif-

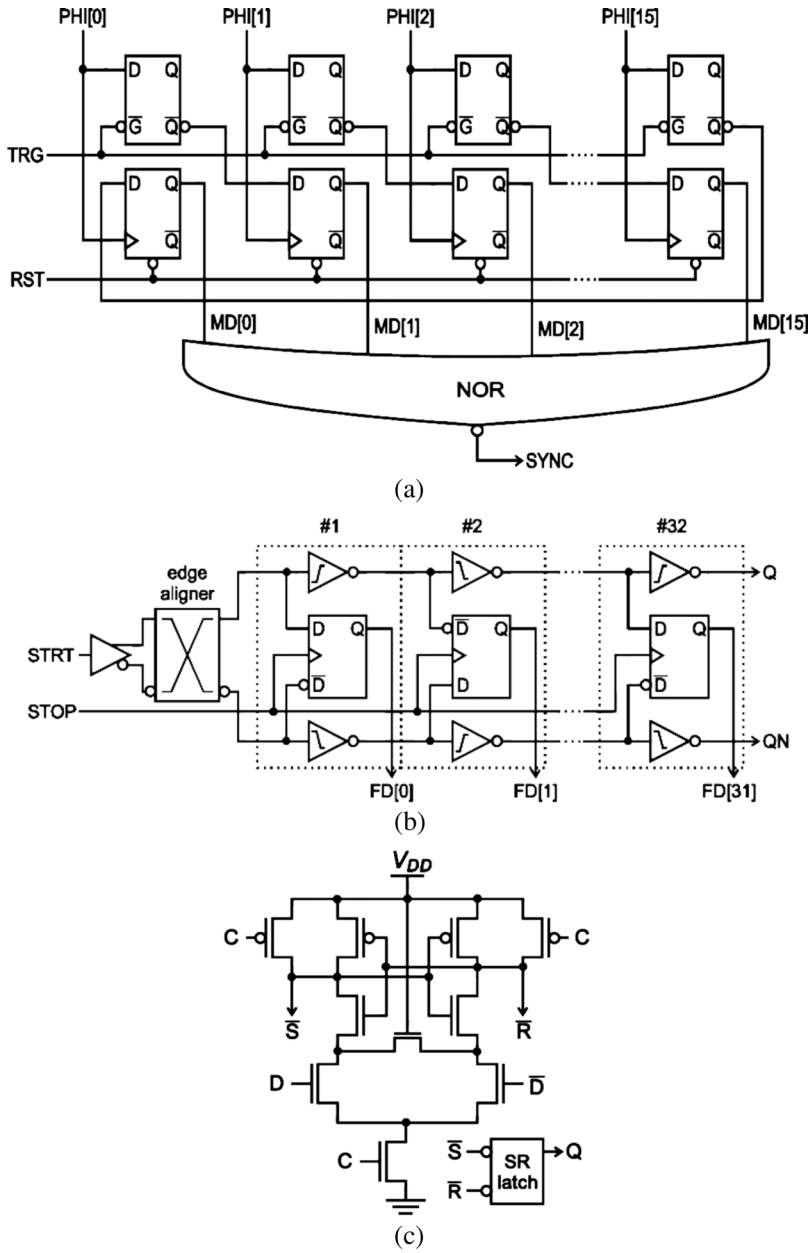

Fig. 5. (a) Medium resolution register and synchronization circuit. (b) Fine delay line and register. (c) Transistor-level schematics of the differential D-flip-flop used as register.

ferential signal propagates through a different chain of inverters. In order to achieve the specified requirement in terms of propagation delay for inverters, used as τ_F, two types of inverters have been utilized: an inverter optimized for low-to-high transitions and an inverter optimized for high-to-low transitions. Each type of inverter is placed in the delay line in such a way that its effective transition occurs during a time interval measurement, according to Fig. 5(b). Although the two inverters are different, their effective propagation times need to match each other. Note that any timing mismatch between them is cancelled out during propagation of two consecutive delay cells. As a result, a potential timing mismatch does not cause a severe degradation in the TDC linearity. In order to sample the state of the propagation of STRT in the delay line, a differential D-flip-flop is used as register, triggered by a STOP (SYNC) signal. The differential flip-flop, shown in Fig. 5(c), is based on a sense amplifier topology and it is symmetric with respect to its data input, similarly to [31] and [33].

Only 16 delay cells (4 bits) of the fine delay line are used for the final result. The remaining delay cells are added to accommodate timing shifts due to PVT variations. In the TDC controller, an interpolator utilizes the three measurements, i.e., coarse, medium, and fine, so as to generate a 10-bit time-to-digital code.

Referring back to Fig. 3(b), when the TDC is in calibration mode, it utilizes the full 32-tap fine delay line in combination with a phase/frequency detector (PFD) and a charge pump (CP) to form a local DLL. In this mode, CALRQ is asserted by the TDC controller which, in turn, connects PHI[i] to TRG via the input multiplexer. The DLL locks to two nonsuccessive phases

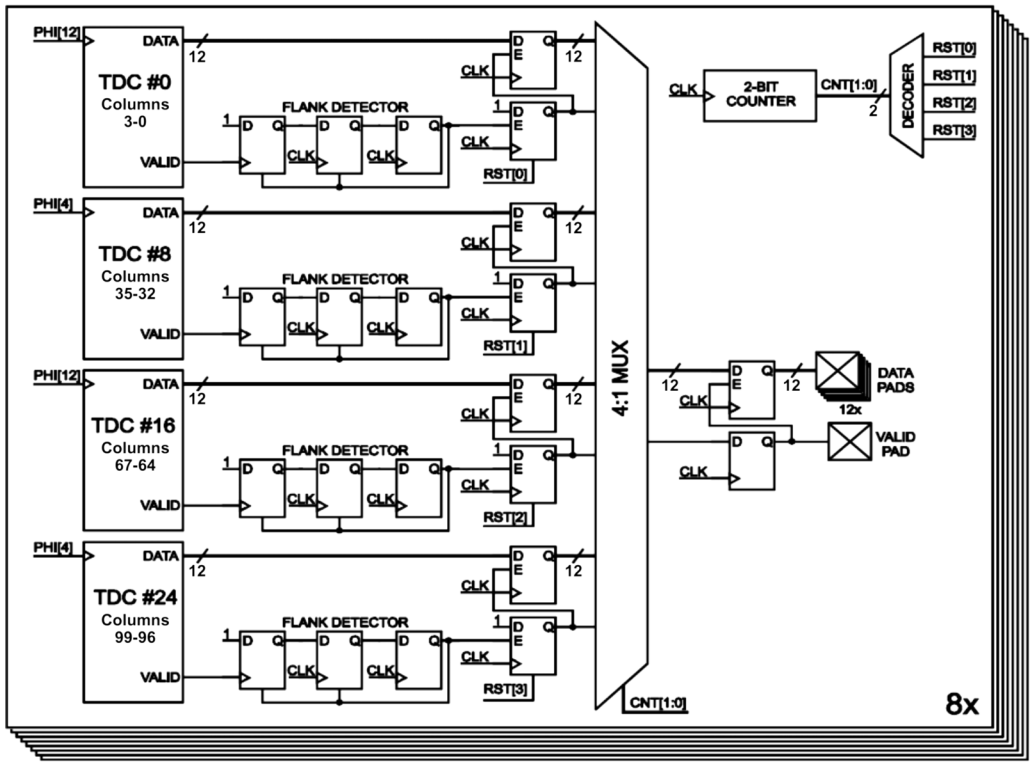

Fig. 6. Simplified block diagram of the readout circuit. The basic circuit is instantiated eight times in the imager so as to read out the data of all the 32 TDCs in parallel.

(PHI[i] and PHI[i+2]) with a total duration of $2\tau_M$, thus generating a fine resolution τ_F of 97.66 ps. The analog control voltage of the DLL is stored on a local capacitor and used in measurement mode. Note that since calibration is performed individually in each TDC, matching requirements between TDCs may be relaxed.

Since every TDC locks to two nonsuccessive global phases PHI[15:0], the main DLL is of high importance. Fortunately, it can be optimized with little or no constraint in silicon area as the imager only has a single instance of it. Moreover, in order to guarantee that every phase line, say PHI[i], is loaded with the same capacitance, the 32 TDCs are distributed evenly among the 16 phases. For instance, reference signal PHI[i] of the 1st and 17th TDCs is PHI[0], whereas the 2nd and 18th TDCs utilizes PHI[1] as reference, the 3rd and 19th TDCs utilizes PHI[2], and so on. Although this scheme requires that the number of TDC is a multiple of the number of phases, it ensures no load mismatches and consequently leads to high timing precision between reference phases.

D. Readout Interface

The output of all TDCs is transferred off-chip via a fast global readout circuit consisting of 32 TDC interface blocks and a pipelined time-multiplexer readout chain. Fig. 6 shows a simplified block diagram of the readout circuit.

In the figure, the basic readout circuit, covering four TDCs, is shown. This circuit is instantiated 8 times on the image sensor so as to read out the data from all the 32 TDCs in parallel. Note that TDC data consist of 12 bits, i.e., two bits to indicate which column out of the four sharing a same TDC the measurement data are for, and 10 bits of actual TDC measurement. Data readout in a given cycle is requested by a TDC via a control signal, called VALID, indicating that valid data are available. TDCs and readout circuit operate in two different clock domains. As a result, every basic readout circuit has a TDC interface circuit so as to handle synchronization issues, as can be seen in Fig. 6. The interface block securely samples the 12-bit data and VALID bit within the readout clock domain. A pipelined time-multiplexer chain transfers the TDC data along with the VALID bit onto a set of digital pads, consisting of one output bus. In order to maximize data rate, the readout circuit operates at a frequency of at least four times faster than the TDC measurement. As a result, every TDC may operate at its maximum throughput. Moreover, as can be seen in Fig. 6, data pads only toggle state when valid data are available in a readout cycle, thus minimizing power consumption.

III. Measurement Results

This design was fabricated in a high-voltage 0.35 μm CMOS technology. The implemented IC was tested and characterized with respect to a number of performance parameters. Basic testing demonstrated full functionality of the design.

A. Single-Photon Imager

Fig. 7 shows a photomicrograph of the IC along with a detail of the pixel. The pitch of the pixel is 25 μm, while the active diameter of the circular SPAD is 7 μm. This design thus leads to an active area fill factor of approximately 6%.

Sensitivity performance of the single-photon imager is characterized by means of photon detection probability (PDP) [25],

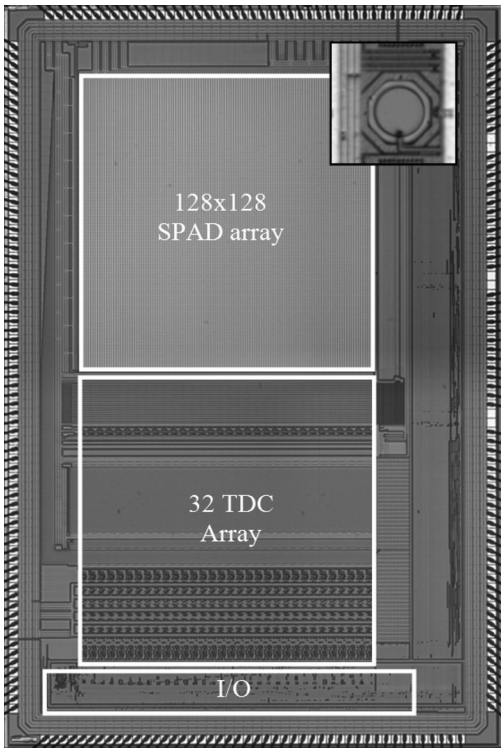

Fig. 7. Photomicrograph of the TCSPC image sensor with a pixel detail in the inset. The integrated circuit, fabricated in a 0.35 μm CMOS technology, has a surface of 8×5 mm^2. The pixel pitch is 25 μm, which leads to an active area fill factor of 6.16%.

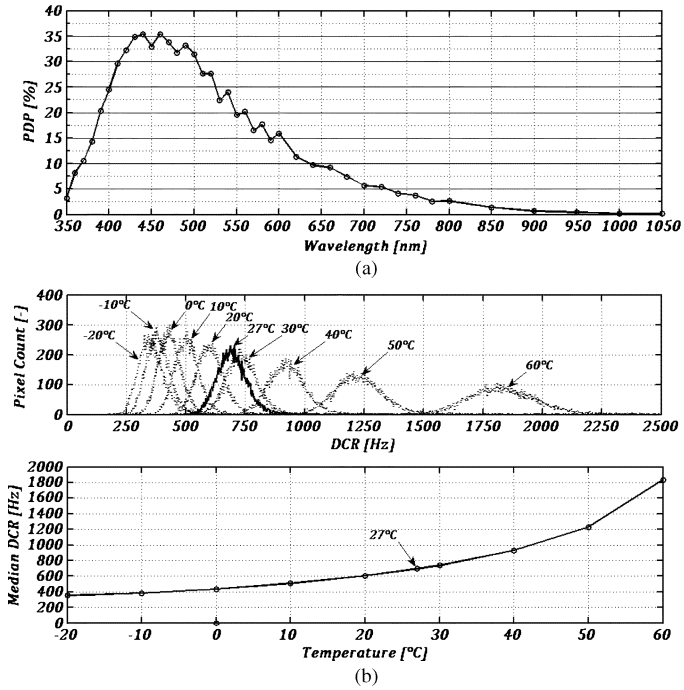

Fig. 8. (a) PDP as a function of wavelength for V_E of 3.3 V. (b) Top: DCR distribution over the array for V_E of 3.3 V and with temperature as a parameter. Bottom: Median DCR as a function of temperature.

a typical measure for SPADs. Fig. 8(a) shows a plot of PDP as a function of photon wavelength, for the nominal V_E of 3.3 V. The maximum value of PDP is 35.4% at 460 nm.

Noise performance is mainly measured in SPAD-based image sensors via its dark count rate (DCR) [25]. Dark counts in SPADs are due to thermally or tunneling generated carriers within its p-n junction, which trigger Geiger pulses that are indistinguishable from regular photon-triggered pulses. DCR is a very important parameter since it defines the noise level in dark condition, thus limiting the detection dynamic range from the low end. Since the mean value of DCR is systematic and may be subtracted from every pixel in most applications, the ultimate noise contribution in SPAD-based image sensors arises from the time-varying component of DCR.

In this paper, thanks to the size of the array, the measurement of DCR distribution over a very high number of Geiger-mode photodiodes became possible, and it is therefore reported for the first time. The DCR distribution over all the 16384 pixels, at several temperatures, is shown in Fig. 8(b). At 27°C, the median value of DCR was 694 Hz whereas the mean value was higher, at 2.4 kHz, mostly due to a small number of highly noisy pixels. In many applications, it is advantageous to electronically ignore these pixels replace them by local averages. As a result, the median value of DCR is a better performance parameter than the mean value. The measured median DCR also stays fairly constant among devices from the same fabrication batch. The median DCR measured at room temperature over a few samples of the design reported in this paper spreads of only 96 Hz, from the best device to the noisiest one considered. As can be seen in Fig. 8(b), the median DCR is a strong function of temperature for temperatures higher than 0 °C. Below this temperature, only limited performance gain is obtained when cooling the device due to the tunneling contribution in DCR. Also visible in Fig. 8(b), the statistical spreading of DCR over pixels increases monotonically with temperature from −20 °C up to 60 °C.

B. Time-to-Digital Converter

The bank of TDCs and associated circuitry were tested and monitored over a number of days of operation. TDC characterization was performed based on differential nonlinearity (DNL). The integral of DNL over all the possible resulting codes of a TDC, i.e., integral nonlinearity (INL), was also computed from DNL measurements. DNL was measured taking advantage of the statistical properties of uncorrelated photons, which follow a Poisson distribution. The stop signal of the TDC under test was connected to a single-photon pixel which, under uncorrelated background light, generated a train of photon-detection pulses with random arrival times. The pixel count rate was adjusted so as to provide a mean arrival time much larger than the TDC measurement range, which was 100 ns in typical condition. Since the TDC stop assertions were random in time with respect to its start signal, the probability of generating a particular TDC code within the measurement range was uniformly distributed. As a result, when a histogram on the generated TDC codes is built using this measurement setup, a uniform histogram is expected for an ideal TDC. However, due to nonidealities within the TDC, some TDC codes account for a longer duration than the ideal TDC resolution and, as a result, those codes have higher probability of capturing events. These nonuniformities are recorded in the resulting histogram. Similarly, TDC codes with shorter duration than the ideal resolution have lower probability of being

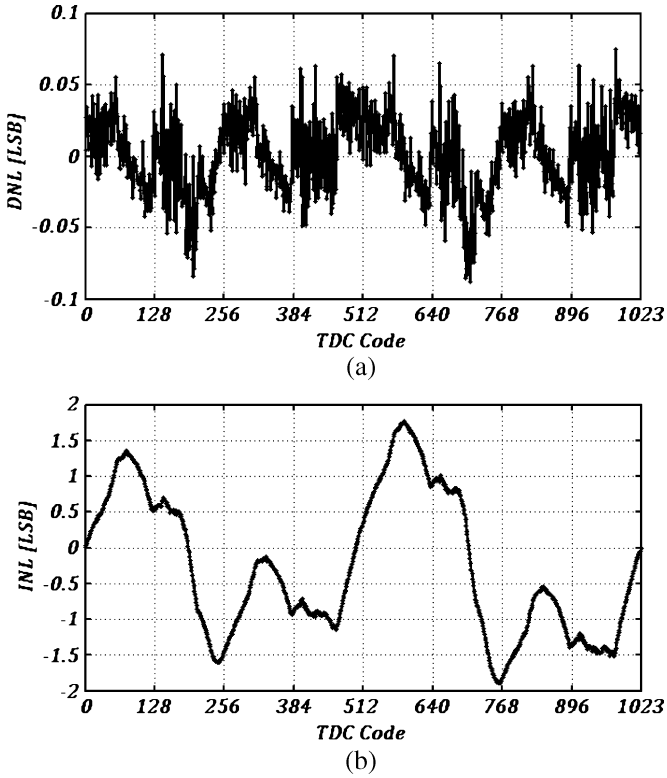

Fig. 9. Measurements of (a) differential nonlinearity (DNL) and (b) integral nonlinearity (INL) for the worst case TDC at room temperature.

triggered by photons and exhibit lower bin values within the histogram. DNL can be consequently extracted from the histogram by comparing every bin value to the ideal expected value. DNL and INL measurements were carried out for all the 32 TDCs. Fig. 9 shows the plot of DNL and INL for a TDC, which was chosen as the worst-case INL among all the 32 TDCs. Due to electrical crosstalk of some TDC signals on periodic digital signals such as clock, the INL response was relatively higher than expected. Its maximum value was 1.89 LSB. Note that since the full TDC range covers 4 clock cycles, DNL and INL exhibited a periodic behavior.

In order to complete TDC testing and characterization, the image sensor was illuminated with a pulsed laser source with a repetition rate of 40 MHz and pulse duration of 80 ps. The trigger out signal of the laser source was used a start signal for the TDCs and as a result, time intervals from laser source to the image sensor could be measured. Fig. 10 shows a histogram of the photon arrival times as recorded using an on-chip TDC. In the picture, a single pulse is shown although the actual histogram comprises four pulses due to TDC range, which is four times longer than the laser period. The full-width at half maximum (FWHM) of the recorded pulse was approximately 250 ps, thus showing some additional jitter components arising from the single-photon pixel and TDC circuitry. As can be seen in the picture inset, where a semi-log plot is shown, the Gaussian shaped component in the jitter measurement indicates a typical circuit jitter contribution. The exponential tail in the recorded pulse on the other hand comes from carrier diffusion times within this SPAD device [6]. Circuit jitter was expected to be an issue due to signal crosstalk between miniaturized pixels and TDCs. Indeed, when all the TDCs are in operation, such as when the measurement of Fig. 10 was performed, digital switching noise is coupled to analog and power signals due to space constraints, which induce timing jitter on some internal signals of the TDCs.

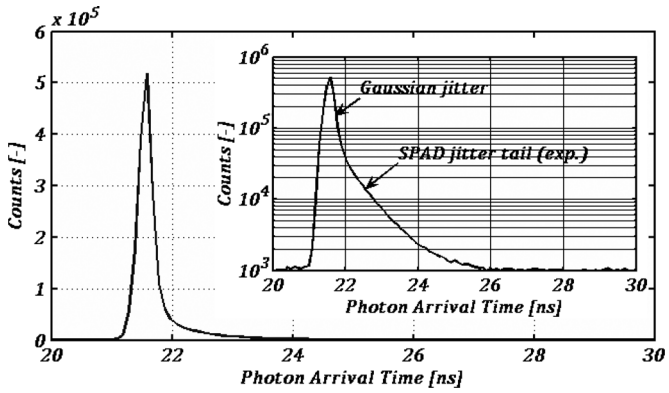

Fig. 10. Time jitter measurement of the SPAD detector and overall circuitry using the integrated TDCs. In the inset, a logarithmic plot is shown.

C. Rangefinder

As a first application, the image sensor was evaluated as a scannerless time-of-flight (TOF) rangefinder based on the time-correlated single-photon counting technique (TCSPC). The measurement setup and associated signal processing used in this work is reported in detail in [32]. TCSPC-based rangefinder involves a pulsed light source used to illuminate the target objects in front of the image sensor. The time taken by light pulses to travel from the source to objects and back to the single-photon sensor, i.e., TOF, is measured using the on-chip TDCs for every pixel. TOF is then converted to distance z as $TOF(c/2)$, where c is the speed of light.

Ranging performance was first quantitatively evaluated by studying distance error versus a reference panel, assumed as ground truth. The reference panel was carefully aligned in front of the sensor and its distance was varied from 40 cm up to 360 cm in steps of 20 cm, using an alternative measuring method. Systematic errors in the alignment and displacement of the reference panel, using the alternative method, were estimated to be within ± 3 mm. A solid-state pulsed laser source emitting an average of 1 mW of optical power at 635 nm was used to illuminate the reference panel. The laser repetition rate was 40 MHz and the duration of light pulses was 80 ps (FWHM). In order to accurately determine TOF, the trigger out signal of the laser source was again used as a reference signal for the IC to lock on. A diffuser was placed in front of the laser source so as to generate a light beam with a field-of-view of 5°. The sensor was equipped with an imaging lens (f/1.4) and with a narrow-band interference filter centered at 635 nm so as to block most of background light. The passband spectral width of the optical filter was 11 nm, enough to accommodate the spectral spread of the laser source around its central emission wavelength. The evaluation of distance precision of our sensor was carried out under a constant 150 lux indoor background. At each evaluation distance, a set of 1000 distance computations was recorded for a pixel at the center of the array, based on an acquisition time of 50

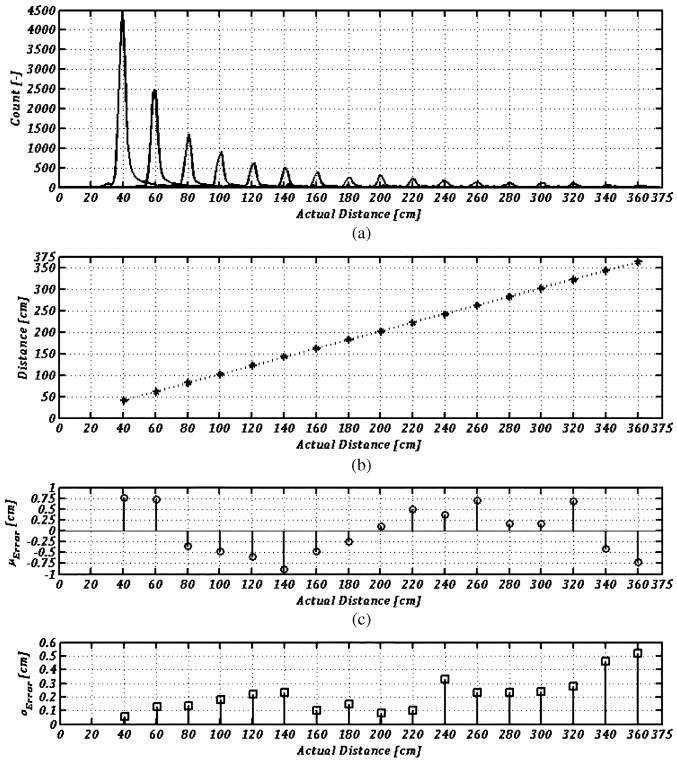

Fig. 11. Rangefinding performance using a 40 MHz pulsed laser source emitting 1 mW of optical power within a field-of-view of 5°. Every distance measurement was based on an acquisition time of 50 ms: (a) histogram curves obtained when moving the target from 40 cm up to 360 cm with steps of 20 cm, (b) measured versus actual distance, (c) mean error with respect to ground truth, and (d) 1σ repeatability errors as a function of distance.

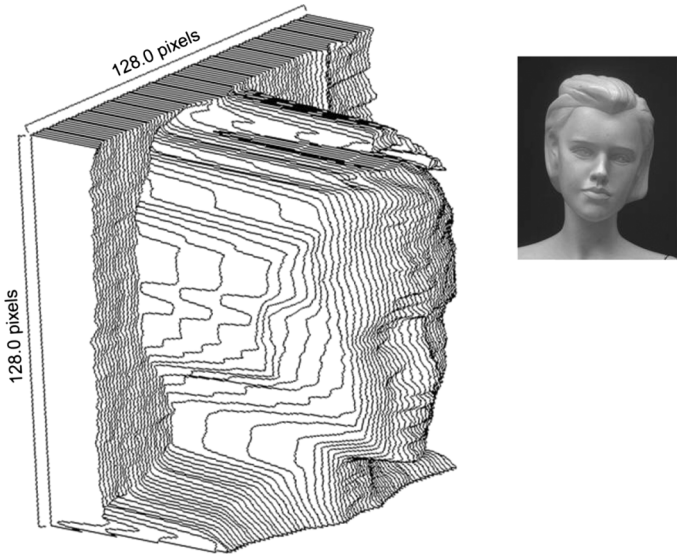

Fig. 12. Experimental 3-D image with model picture in inset. Measurement based on a target distance of 1 m and on an illumination field-of-view of 30°. Remaining parameters kept unchanged.

ms per point. Fig. 11 shows a set of plots summarizing ranging performance. At the top graph of Fig. 11, a sample histogram for each distance step is plotted, based on the mentioned measurement conditions. As can be seen, the bandpass optical filter was effective in eliminating uncorrelated photons. Remaining background photons falling on the laser emission spectral band and possible dark counts are distributed evenly over the full histogram and therefore have a negligible impact on the signal peak [32], accurately built around each distance. A quadratic decrease in signal peak as a function of distance is clearly visible due to the light source field-of-view. However, as can be seen in the second plot of Fig. 11, where mean measured distance as a function of actual distance is plotted, a few tens of photons are enough to accurately determine distance. The mean distance error μ_{Error} among the set of 1000 measurements at each distance as well as its standard deviation σ_{Error} are plotted at the bottom of Fig. 11. The maximum μ_{Error} was within ± 9 mm over the full range, whereas the maximum time-varying uncertainty σ_{Error} at each distance was 5.2 mm. μ_{Error} is mostly due to TDC nonlinearity, while a fraction of it may be explained by the systematic uncertainty of ± 3 mm in aligning the reference panel. At short distances, μ_{Error} was also believed to be impaired by signal crosstalk within the lens cavity due to sensor-to-lens and lens-to-sensor multireflections. These effects become negligible at longer distances as the number of incident photons reduces strongly. Conveniently, since the signal peak spreads over at least 7 bins in the histogram, the effects of TDC nonlinearity and some quantization errors were attenuated, thus leading to an μ_{Error} lower than 9 mm. When taking into account the limited 1 mW of average optical power and 50 ms of acquisition time, σ_{Error} performance favorably compares with the state-of-the-art. Towards the end of the distance range, the number of photons detected per histogram was only a few tens and as a result, photon shot-noise resulted in increased single-shot distance uncertainty.

Finally, the fully integrated rangefinder sensor was qualitatively evaluated by taking a depth snapshot of a human-size mannequin face. The model was placed at 1 m from the sensor. In order for the light source to illuminate the model completely, a diffuser inducing a field-of-view of 30° was installed. Fig. 12 shows the depth map result of the model as well as the picture of the model, captured with a standard digital camera.

IV. Conclusion

We have presented the first fully integrated system for single-photon time-of-arrival evaluation. The IC comprises an array of 128×128 single-photon avalanche diodes with active recharge, a bank of 32 independent TDCs, and a 7.68-Gbps readout system. The 32 converters are shared among 128 detectors in a line using an event-driven scheme. A continuously operating calibration scheme ensures an individual resolution of 97 ps within 100 ns of range and over a wide range of temperatures. The bank of converters can perform a total of 320 million single-photon time-of-arrival evaluations per second.

Device characterization showed a maximum photon detection probability of 35% at 460 nm in typical conditions. Device noise performance was reported via a measurement of dark count rate distribution over the array. This measurement was performed over different temperatures and using a number of IC samples. The median dark count rate across all the devices in a sensor was 694 Hz at 27 °C and its peak-to-peak spreading over different

TABLE I
PERFORMANCE SUMMARY

	Parameter	Symbol	Min.	Typ.	Max.	Unit
Pixel	Photon detection probability @ V_E=3.3V	PDP			35 @ 460nm	%
	Sensitivity spectrum	λ	350		800	nm
	Median DCR at 27°C of temperature	DCR	598	646	694	Hz
	Dead time	τ_{DT}		100		ns
TDC	Tuning of measurement range (10 bits)		71.68	100	204.8	ns
	Resolution (LSB)	τ_F	70	97.66	200	ps
	Measurement rate				10	MS/s
	Maximum DNL			0.08		LSB
	Maximum INL			1.89		LSB
System	Clock frequency (DLL locking range at room temperature)		19.5	40	55.8	MHz
	Total IO bandwidth at 80MHz			7.68		Gbps
	JTAG bandwidth			8		Mbps
	Static power dissipation			33		mW
	Dynamic power dissipation			150		mW
Illumination System	Average power			1		mW
	Peak power			250		mW
	Repetition rate			40		MHz
	Duty cycle			0.4		%
	Wavelength			635		nm
Rangefinding Performance	Acquisition time			50		ms
	Distance range (40Mhz)		20		375	cm
	Maximum mean error w.r.t. reference[1,2]			9		mm
	Maximum error standard deviation[1,2]			5.2		mm

[1] Statistical measurement based on 1000 samples at each distance considered.
[2] Reference measured with an uncertainty of approximately ±3 mm.

sensors was within a range of 96 Hz. The statistical median assessment as an alternative to the simple mean value showed to be a more reliable measure to compare performance of SPAD arrays among different IC samples and different operating conditions. Indeed, the mean dark count rate value revealed to be impractical as it carried a very important random component due to a small number of extremely noisy pixels, which in most cases may be considered as defects.

This design has enabled us to reconstruct 3-D scenes with milimetric precisions in extremely low signal exposure. A laser source was used to illuminate the scene up to 3.75 m with an average power of 1 mW, a field-of-view of 5°, and under 150 lux of constant background light. Accurate distance measurements were repeatedly achieved based on a short integration time of 50 ms even when signal photon count rates as low as a few hundred photons per second were available. The maximum nonlinearity

in distance measurement was 9 mm over the full measurement range. Time-varying uncertainty at the farthest distance was 5.2 mm. We believe that, while time-varying uncertainty has limited improvement potential under the same illumination power budget, nonlinearity errors may be effectively improved with lower TDC nonlinearity and/or with parameterized nonlinearity compensation. Other applications, beyond optical rangefinding, include fast fluorescence lifetime imaging, particle imaging velocimetry, fluorescence correlation spectroscopy, etc.

ACKNOWLEDGMENT

The authors are grateful to M. Sergio for help during the IC tape-out and to F. Monnier for help in the experimental evaluation of the sensor performance when operated as a rangefinder.

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