High Speed CMOS Imaging: Four Years Later
(INVITED)

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Abstract– *Four years ago [1] we assessed the status of CMOS imaging for high-speed applications. We also gave an outlook of the near future in high-speed imaging. In this paper we revisit the topic of high speed imaging in a slightly different angle and make the point of recent developments in the field, with emphasis to bioimaging applications.*

Introduction

In recent years, the pressure on imagers to become faster and better performing has further accelerated. Well-known techniques, such as TCSPC, requiring sub-nanosecond photon detection resolutions have registered an important growth. Other applications, such as time-of-flight (TOF) based 3D vision, have become more mature and very promising.

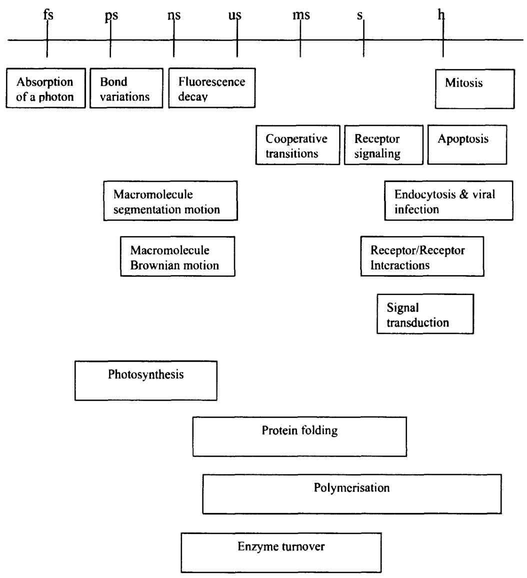

Fig. 1. Time scales for various bio-processes (Source: [2]).

In the field of bioimaging in particular, speed and sensitivity have become the main differentiator in analyses that were simply not possible until a few years ago. Fig. 1 shows the time scales for some of the most important biological processes today [2]. Not all the processes in Fig. 1 can be captured with an optical system, at least directly, however, many of them are characterized today with optical means.

Even when the process is inherently slow, optical techniques, such as fluorescence lifetime imaging microscopy (FLIM), Förster resonance energy transfer (FRET), and fluorescence correlation spectroscopy (FCS), make use of photon counting imagers, possibly with femto and picosecond accuracies [3],[4],[5],[6],[7].

Among the applications for high-speed imaging reviewed in [1], we listed high-speed video, free-space communications, geo surveying, face recognition, *in vivo* brain analysis, transillumination, in addition to FLIM, FRET, and FCS. Today, fluorescence based imaging is arguably the dominant force behind the development of fast imagers, while other applications, such as brain analysis, face recognition, and telecommunications have somewhat faded. Emerging applications, currently gaining traction, are 3D imaging based on TOF, particle image velocimetry (PIV), molecular and medical imaging, internal combustion engine optimization, and high-speed video for consumer uses.

3D imagers have reached considerable maturity with the establishment of entire lines of commercial products and their announced use in automotive safety, security, and monitoring applications [8].

PIV systems [9], thanks to novel computer vision algorithms, are now increasingly used in geo surveying and weather pattern analysis, as well as in natural phenomena monitoring and hazard warning systems.

The field of optical imaging with nanometer resolution and optical molecular imaging are two of the fastest growing fields of research today, often interacting with medical imaging disciplines. Medical imaging is

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currently expanding beyond digital X-ray imaging [10], into new fields whereby optical, ultrasound, and magnetic resonance imaging intersect.

Energy efficiency is another field where unconventionally fast and robust imagers might become an important ingredient. In [11] for example the authors advocate the use of a high-speed camera to monitor internal combustion. Computer vision techniques could in principle enable the creation of a feedback loop for the optimization of the combustion parameters.

High-speed video for consumer applications is especially used in optical computer mouse devices and gaming interfaces. In this context, it is likely that future demands of the videogame industry will have an impact on the requirements of imager speed.

New human-computer interfaces (HCIs) based on conventional 2D cameras, and that could easily be extended to 3D cameras, have recently moved from the research arena to mainstream. However, the preferred user interfaces are still keyboards, albeit based on a touch-screen. Hence it is not clear whether 3D cameras will be used to solve HCI specific problems.

In the remainder of the paper we look at a type of detectors, known as single-photon avalanche diodes (SPADs), where significant advances have recently been made to enable high speed operation and high resolution timing resolution at the pixel basis. In this context we focus on labs-on-chip (LoCs) and micro total analysis systems (μTAS).

SPAD Imagers

LoC and μTAS applications require not only a high level of miniaturization but also high reliability, high sensitivity, and low power. We have advocated the importance of high speed as well and this is why system integration is often used to achieve these goals.

In [1] SPAD technology was presented as a potential replacement for micro- or multi-channel plates (MCPs) [12] for time-correlated sensing platforms, especially in LoCs and μTASs, whereby miniaturization and low power consumption are the most important goals. While the use of SPADs as time-correlated detectors with picosecond uncertainty was recognized decades ago [13], it was the introduction of SPADs fabricated in CMOS, that made it feasible to build large imaging devices [14],[15].

Since 2004 several developments made SPADs even more attractive to achieve high levels of miniaturization while exhibiting low photon timing uncertainty and excellent noise performance. Several research groups are now active in the field of CMOS SPAD design. The intense research effort has resulted in pitch reduction, density increase, and detection cycle reduction. We were the first to propose large arrays of SPADs [16],[17]. We also proposed the first SPADs implemented in deep submicron CMOS processes [18],[19].

Effort has also been devoted to the design of imagers, with emphasis to readout architectures aimed at the minimization of dead time and the maximization of dynamic range [20],[21],[22]. The first fully integrated SPAD sensor with time discrimination circuitry was recently introduced [23]. This design is currently the largest SPAD array in any technology and the one with the highest SPAD density ever achieved.

SPAD arrays have been used by other authors for a variety of applications, including 3D imaging, bioimaging, micro-assays, etc., in several CMOS processes [24],[25],[26],[27],[28]. Other authors have proposed the use of dedicated technologies to optimize SPAD noise performance. The literature on the subject is extensive, see [29] for a review. Hybrid solutions have also been proposed to take advantage of the best technology for the detector and ancillary electronic circuits, such as the time discriminator. An example of this approach can be found in [30].

Tab. 2 shows a summary of the performance measurements relevant for SPADs and SPAD imagers. The data reported here are obtained from published and accepted material.

Measurement	Min	Typ	Max	Unit
Fill factor	1		10	%
Timing uncertainty	50		145	ps
DCR	5		780	Hz
Pixel pitch	20		58	μm
V_{OP}	10		23	V
Dead time		40		ns
PDP @ 550nm		41		%
EM spectrum	380		900	nm
Saturation count		25		MHz

Tab. 2. Typical performance of currently available SPADs.

Imager Miniaturization for LoC and μTAS

The first SPAD implementations in 0.35μm CMOS technology have demonstrated fully scalable pixels at a pitch of 25μm. Pixel miniaturization has other benefits too. For example, due to a reduced number of charges involved in the avalanche effect, electrical and optical crosstalk may be reduced. Afterpulsing probability may also be reduced for the same reasons, thus possibly enabling designers to trade it off for dead time.

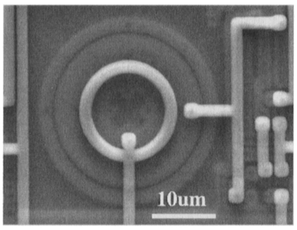

Fig. 3. SPAD implementation in CMOS: SEM micrograph.

Fig. 3 shows a possible implementation of a SPAD that ensures compatibility with conventional CMOS processes thanks to a properly biased quenching transistor and an inverter used for pulse shaping [17].

SPAD arrays can also be used for multi-photon detection when connected as an *N*-to-1 OR gate or a current summing device. This configuration can be achieved effectively, for example, with the schematic shown in Fig. 4.

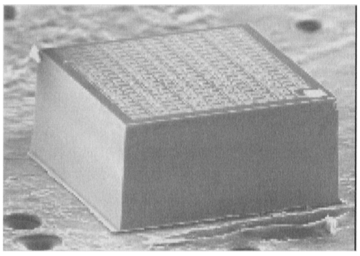

Fig. 4. Integrated avalanche photodiode array in common anode configuration, known as *silicon photomultiplier* (Courtesy of SensL).

When the SPAD array operates as an imager, the main challenge is readout. Since SPADs may generate a digital pulse for each absorbed photon, to avoid missing photon counts, a counter can be used in each pixel [31]. However, large counters are not desirable due to the fill factor loss and/or extra time required to perform a complete readout of the contents of the chip. A partial solution to this problem is the reduction of the counter resolution (ultimately 1 bit), requiring more frequent readouts and/or lower saturation.

Another solution is to access every pixel independently but sequentially using a digital random access scheme [17]. In low-light-level (LLL) applications, such as in bioluminescence setups, one can use an *event-driven* readout, where the detector initiates and drives a column-wise detection process directly [18],[20].

An alternative approach for non-LLL situations is the use of a *latchless pipeline* scheme [21]. In this approach, the absorption of a photon causes the SPAD to inject a digital signal onto a delay line that is then read externally.

Combining optical detection and other functionalities on the same substrate for LoC and μTAS applications is also being researched quite extensively. Among the most promising developments, Lehmann *et al.* have proposed the use of SPADs integrated on the same substrate with magnetic actuation devices [32]. In this work, single-photon detectors were selected due to their high dynamic range, necessary to detect small particles in a condition of high illumination. In addition, the insensitivity of *in situ* SPADs to magnetic fields and humidity made them ideal for use in wet environments with magnetically actuated bio-material. More recently, Brae *et al.* have proposed a μTAS whereas a micro LED array operating in near UV is bump-bonded to a CMOS SPAD array [33]. In this work, a time-correlated single-photon counting (TCSPC) based setup is used without dichroic filters to measure the lifetime of quantum dots for uses in bioimaging applications.

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