Thermal Analysis of 3D Integrated Circuits Based on Discontinuous Galerkin Finite Element Method

Amir Zjajo, Nick van der Meijs, Rene van Leuken Circuits and Systems Group, Delft University of Technology Mekelweg 4, 2628 CD Delft, The Netherlands

Abstract

Even though vertical 3D integration offers increased device density, reduced signal delay, and design flexibility, heat and thermal concerns are, nevertheless, aggravated. In this context, accurate computation of temperature profile is required to establish thermal design rules governing the feasibility of integration options. Within this framework, a novel methodology based on discontinuous Galerkin finite element method for accurate thermal profile estimation of 3D integrated circuits is proposed[§]. The method is utilized to simulate geometrically complicated physical structures with limited complexity overhead.

Keywords

CAD, Thermal analysis, 3D IC, Multi-layer, Simulation, Adaptive error control

1. Introduction

In the nanometer regime, the transistor scaling has been slowing down due to the challenges and hindrances of increasing variability, short-channel effects, power/thermal problems and the complexity of interconnect. The 3D integration has been proposed as one of the alternatives to overcome the interconnect restrictions [1]. However, thermal management is of critical importance for 3D IC designs [2] due to the degradation of performance and reliability [3]. Heat and thermal problems are exacerbated for 3D applications as the vertically stacked multiple layers of active devices cause a rapid increase of power density. Higher temperature increases the risk of damaging the devices and interconnects (since major back-end and frontend reliability issues including electromigration, timebreakdown, dependent dielectric and negative-bias temperature instability have strong dependence on temperature), even with advanced thermal management technologies [4]. The complexity of the interconnection structures, back end of line structures and through-silicon vias increase the complexity of the conductive heat transfer paths in a stacked die structure. Dummy vias and inter-tier connections can be used to increase the vertical heat transfer through the stack and reduce the temperature peaks in the die [5]. Additionally, the thermal conductivity of the dielectric layers inserted between device layers for insulation is very low compared to silicon and metal [6] leading to temperature gradient in the vertical direction of a 3D chip. In the case of hot spots, these thermal effects are even more pronounced.

Successful application of 3D integration requires analysis of thermal management problem and the development of an analytical model for heat transport in 3D ICs to establish thermal design rules governing the feasibility of integration options. A thermal analysis of heterogeneous 3D ICs with various integration schemes has been presented in [7]. The analysis of temperature distribution on an inhomogeneous substrate layer is performed employing finite-difference time domain [8], based on the image method [9], neural networks, [10], green function [11], fast Hankel transform of green function [12], or mesh based methods [13]. However, existing thermal-simulation methods, when applied to a fullchip, reduce the computational complexity of the problem by homogenizing the materials within a layer, limiting the extent of an eigenfunction expansion, or ignoring sources' proximity to boundaries. These simplifications render their results less accurate at fine length-scales, on wires, vias, or individual transistors.

Accurate computation of temperature at the length-scales of devices and interconnects requires the development of a fundamental analytical model for heat transport in 3D ICs and a detailed accounting of the heat flow from the powersources through the nanometerscale layout within the chip. In this paper, we propose thermal conduction model with boundary condition residuals and a methodology based on discontinuous Galerkin finite element method for accurate thermal profile estimation of a circuit components in 3D multi-layer substrate. The method provides both, steady-state and transient 3D temperature distribution and can be utilized to simulate geometrically complicated physical structures with limited complexity overhead.

2. Thermal analysis model and algorithms

In order to accurately estimate on-chip thermal gradients, a temperature profile estimation methodology is proposed with the capability to include layout geometry of individual circuit blocks in a chip (Figure 1). The chip is partitioned into a mesh according to the information provided by the layout geometry. Physical parameters such as thermal conductivity and heat transfer coefficient depend on specific packaging material properties and applied cooling techniques. Boundary conditions are determined by the operating environment. The simulator uses layout geometry, boundary conditions, and physical thermal parameters as initial values to formulate the system of partial differential equations (PDEs), which are approximated into a system of ordinary differential equations (ODEs) with discontinuous Galerkin method. The ODEs are then numerically integrated in a self-consistent manner using modified Runge-Kutta method.

[§] This research was supported in part by the CATRENE program under the Computing Fabric for High Performance Application (COBRA) PROJECT CA104.



Figure 1: The methodology for thermal profile estimation

The electrothermal couplings are also embedded in the core of the simulator that simultaneously estimates temperature-dependent quantities for each simulation step.

2.1. Thermal conduction in integrated circuits

Fundamentally, IC thermal modeling is the simulation of heat transfer from heat producers (transistors and interconnect), through silicon die and cooling package, to the ambient environment. A schematic representation of the chip layer and its thermal mesh model is shown in Figure 2. The chip is divided into meshes evenly in the x, y, and z directions, here, δx , δy and δz are each mesh's side sizes. The equation governing heat diffusion via thermal conduction in an IC follows

$$c_v \,\partial T_i / \partial t + \operatorname{div}[\mathbf{g}(\operatorname{grad} T)^T] - Q = 0 \tag{1}$$

where Q is the heat source, T is the temperature at time t, c_V is a capacitance of the volume V, $\operatorname{grad} T = [\partial T / \partial x, \partial T / \partial y]$ $\partial T/\partial z$], and the matrix g is the conductivity matrix of the material. For materials that have three orthogonal directions of different thermal conductivities $g=\text{diag}(g_i), i=x,y,z, g_y, g_y$ and g_z are the thermal conductivities coefficients. In order to approximate the solutions of these equations using numerical methods, we use finite discretization, i.e., an IC model is decomposed into numerous three-dimensional elements, where adjacent elements interact via heat diffusion. Each element is sufficiently small to permit its temperature to be expressed as a difference equation, as a function of time, its material characteristics, its power dissipation, and the temperatures of its neighboring elements. The temperature in the control volumes along the boundaries of the computational domain is determined using constraints representing boundary conditions. Each cell is assigned the specific heat capacity of the associated material and also a temperature. If a dual grid is formed by joining the centers of adjacent cells, each edge of the dual grid will intersect exactly one face of the primary grid. The thermal conductivity can be thought to be assigned to the edge of the dual grid. If the two cells on either side of the face belong to the same material, the assigned thermal conductivity is that of the material.



Figure 2: (a) The chip top view, (b) 3D view of the grid point *i*, and (c) disk of thickness Δz representing temperature spread

If the two cells belong to different materials, the thermal conductivity is chosen on the basis of the thermal conductivity values of both the materials. We also allow for the existence of interfacial thermal resistance (due to scattering of thermal carriers at the interface).

2.2. Simplified thermal conduction model with surface boundary condition residuals

We take up the Galerkin finite element discretization for the thermal conduction initial boundary value problems. Balancing the order of differentiation by shifting one derivative from the temperature to the test function η is beneficial: we use basis functions that are less smooth since we do not require the second derivatives, and also we are able to satisfy the natural boundary conditions without having to include them as a separate residual. The integration by parts in the case of a multidimensional integral is generalized in the divergence theorem and adding the surface (Newton) boundary condition residual

$$\int_{V} \eta c_{V} \, \partial T_{i} / \partial t \, \mathrm{d}V + \int_{V} (\operatorname{grad} \eta) \boldsymbol{g} (\operatorname{grad} T)^{T} \, \mathrm{d}V - \int_{V} \eta Q \, \mathrm{d}V + \int_{S} \eta h (T - T_{a}) \, \mathrm{d}S = 0 \qquad \eta(\boldsymbol{x}) = 0 \text{ for } \boldsymbol{x} \in S$$
(2)

where T_a is the known temperature of the surrounding medium and h is the surface heat transfer coefficient defined as $h=1/(A_{eff}R)$, where A_{eff} is the effective area normal to the direction of heat flow and R is the equivalent thermal resistance. We assume a Dirichlet boundary condition of the form T=0 (absolute temperature equal to ambient temperature) at the radial and the $z=\max(z)$ boundaries. This condition is applied by setting the temperature at the center of the boundary cells along the radial and the $z=\max(z)$ boundaries to 0. The boundary condition at $z=\min(z)$ is assumed to be of the mixed type $g_z\partial T/\partial z - hT=0$, where g_z is the thermal conductivity in the z direction. Physically, this corresponds to heat loss being proportional to the difference between the absolute temperature and the ambient temperature.

To simplify the problem, we reduce the originally threedimensional model to two active coordinates, while still describing the heat conduction through a three-dimensional domain; the function describing the temperature distribution depends only on two spatial coordinate variables though. Figure 2c) shows a disk of thickness Δz representing temperature spread. If the component of the temperature gradient along the z direction is negligible, $\partial T/\partial z \approx 0$, a necessary condition for the formulation of a simplified model is met. The surface of the three-dimensional solid consists of the two cross sections, and of the cylindrical surfaces, the inner and the outer. The two cylindrical surfaces may be associated with boundary condition of any type. Since the temperature does not vary with z, the integrals in (2) may be simplified by preintegrating in the thickness direction, $dV = \Delta z dS$ and $dS = \Delta z dC$. The volume integrals are then evaluated over the cross-sectional area S_c ; provided h is independent of z. The surface integrals are computed as integrals over the contour of the cross-section C_c as

$$\int_{S_{c}} \eta c_{V} \, \partial T_{i} / \partial t \, \Delta z dS + \int_{S_{c}} (\operatorname{grad} \eta) \boldsymbol{g} (\operatorname{grad} T)^{T} \, \Delta z dS$$

$$- \int_{S_{c}} \eta Q \Delta z dS + \int_{C_{c}} \eta h (T - T_{a}) \Delta z dS = 0 \quad \eta(\boldsymbol{x}) = 0 \text{ for } \boldsymbol{x} \in C_{c}$$
(3)

The thickness Δz is a constant and could cancel without any effect on the solution. Nevertheless, (3) still applies to a fully three-dimensional body. To maintain this notion throughout the paper, we shall not cancel the thickness.

The domain of the surface is approximated as a collection of triangles. As an illustrative example we show in Figure 3 L-form wire. As the triangles are the finite elements with straight edges we are only approximating any boundaries that are curved. This error is controlled by *l*-adaptive error control (see Section 2.4). Because the basis on the standard triangle satisfies the Kronecker delta property, the values of the degrees of freedom $T_i(t)$, $i=1,..., N_j$, at the *i* nodes are simply the values of the interpolated temperature at the nodes, $T_i(t)=T(x_i, y_i, t)$.

The system of ordinary differential equations (ODEs), which results from the introduction of the Galerkin finite element test function η (the so-called discretization in space) on (3) reads

$$\sum_{i=1}^{N_f} C_{ji} \,\partial T_i / \partial t + \sum_{i=1}^{N_f} G_{ji} T_i = L_{Q_j} + L_{\overline{C}_j} + L_{\overline{G}_j}, \quad j = 1, \dots, N_f$$
(4)

where

$$C_{ji} = \int_{S_c} N_{(j)} c_{\nu} N_{(i)} \Delta z dS$$

$$G_{ji} = \int_{S_c} (\operatorname{grad} N_{(j)}) hg(\operatorname{grad} N_{(i)})^T \Delta z dS$$

$$L_{Q_j} = \int_{S_c} N_{(j)} Q \Delta z dS$$
(5)

 C_{ji} , G_{ji} , denote capacity and conductivity matrices, respectively, and L_{Qi} designate internal heat generation.

A. Zjajo, Thermal Analysis of 3D Integrated Circuits



Figure 3: Surface approximation of L-form wire with collection of triangles

Boundary condition in a weighted residual sense is given as

$$L_{\overline{C}_{j}} = -\sum_{i=N_{f}+1}^{N} \left[\int_{S_{c}} N_{(j)} c_{V} N_{(i)} \Delta z dS \right] \partial T_{i} / \partial t$$

$$L_{\overline{G}_{j}} = -\sum_{i=N_{f}+1}^{N} \left[\int_{S_{c}} (\operatorname{grad} N_{(j)}) h \boldsymbol{g} (\operatorname{grad} N_{(i)})^{T} \Delta z dS \right] T_{i}$$
(6)

2.3. Modified Runge-Kutta solver

The ODE in (4) need to be numerically integrated in time as analytical solutions are not possible in general. Although many time marching numerical methods for solving ODEs are based on methods that do not require explicit differentiation, these methods are conceptually based on repeated Taylor series expansions around increasing time instants. Revisiting these roots and basing time marching on Taylor series expansion allows element-by-element time step adaptation by supporting the extrapolation of temperatures at arbitrary times.

We firstly designate numerical dissipation and boundary condition terms and treat them separately. We adopt a more stable semi-implicit treatment of the numerical dissipation terms, which is formally correct for the Crank-Nicolson scheme, but implies a modification of dissipation terms in (4) for the Runge-Kutta scheme. Rewriting the spatially discrete system in (4) as

$$\partial \hat{T} / \partial t = G(T) - \Gamma(T)\hat{T}$$
⁽⁷⁾

where $\Gamma(T)\hat{T}$ denotes the numerical dissipation term, the predictor-corrector scheme is

$$\overline{T}^{*} = \overline{T}^{n} + \Delta t \overline{G}(T^{n})$$

$$(1 + \Delta t \Gamma(T^{n})) \widehat{T}^{*} = \widehat{T}^{n} + \Delta t G(T^{n})$$

$$\overline{T}^{n+1} = 1/2 (\overline{T}^{n} + \overline{T}^{*} + \Delta t \overline{G}(T^{n}) + \Delta t \overline{G}(T^{*}))$$

$$(1 + 1/2 \Delta t \Gamma(T^{*})) =$$

$$= 1/2 (\widehat{T}^{n} + \widehat{T}^{*} + \Delta t G(T^{n}) + \Delta t \overline{G}(T^{*}) - \Delta t \Gamma(T^{*}) \widehat{T}^{n})$$
(8)

for two time instants T^n and T^{n+1} . Note that terms designating boundary conditions are treated separately.

In the proper Crank-Nicolson scheme the state T^* is replaced by T^{n+1} except the last T^* in the last equation, which is replaced by T^n . Utilizing a discontinuity detector as in [14], using T^* in this last case favors stability, because it disallows Γ to be applied at different locations on the left and righthand side. The modified third order Runge-Kutta scheme reads

$$\overline{T}^{(1)} = \overline{T}^{n} + \Delta t \overline{G}(T^{n})
(1 + \Delta t \Gamma(T^{n})) \widehat{T}^{(1)} = \widehat{T}^{n} + \Delta t G(T^{n})
\overline{T}^{(2)} = 1/4 (3\overline{T}^{n} + \overline{T}^{(1)} + \Delta t \overline{G}(T^{(1)}))
(1 + 1/4 \Delta t \Gamma(T^{(1)})) \widehat{T}^{(2)} = 1/4 (3\widehat{T}^{n} + \widehat{T}^{(1)} + \Delta t G(T^{(1)}))
\overline{T}^{n+1} = 1/3 (\overline{T}^{n} + 2\overline{T}^{(2)} + 2\Delta t \overline{G}(T^{(2)}))
(1 + 2/3 \Delta t \Gamma(T^{(2)})) \widehat{T}^{(n+1)} = 1/3 (\widehat{T}^{n} + 2\widehat{T}^{(2)} + 2\Delta t G(T^{(2)}))$$

To achieve fast convergence the coefficients in the Runge-Kutta scheme have been optimized to damp the transients in the pseudo-time integration as quickly as possible and to allow large pseudo-time steps. In addition, the use of a point implicit Runge-Kutta scheme ensures that the integration method is stable. Convergence to steady state is further accelerated using a multigrid technique, e.g. the original fine mesh is coarsened a number of times and the solution on the coarse meshes is used to accelerate convergence to steady state on the fine mesh. A rough time step estimate is based on the characteristics of (9)

$$\Delta t = CFL \min(|S_i|) / \max(\overline{T_i^n} + \hat{T_i^n}, \overline{T_i^n} - \hat{T_i^n})$$
(10)

with *CFL* the Courant-Friedrichs-Lewy number; *CFL* \leq 1 and *i*=1,...*N*_{node}., where *N*_{node} is the total number of nodes. The time step can thus vary over time.

The boundary conditions of (4) and (6) also have to be written in terms of the discrete (in space and time) temperature. For the time-marching between time indices T^n and T^{n+1} , the form of the right-hand side depends, among other things, on the time-marching scheme chosen. The terms involved in the surface integral involve temperature and the spatial derivatives of temperature on the surfaces. We approximate these terms using the nearest neighbor temperatures only. Hence, the discrete form of the surface integral is of the form of a linear combination of the temperature at the center of the cell and the temperature at the center of the neighboring cells.

The modified implicit Runge-Kutta scheme can not be used to compute neighbor temperatures at boundary condition, as it results in circular dependency problems. More specifically, T^n must be know before T_i is computed. Similarly, T^n depends on T_i . To solve this problem, we use the forward Euler method to extrapolate T^n . Additionally, to increase efficiency, we employ backward Euler (θ =1, where the free parameter θ is used to control accuracy and stability of the scheme) and factor the matrix L_Q before the time stepping starts and then use forward and backward substitution in each time step

$$\theta[L_{\overline{C},j}]^{n+1} + (1-\theta)[L_{\overline{C},j}]^{n+1} = -\sum_{i=N_{f}+1}^{N} \left[\int_{S_{c}} N_{(j)} c_{V} N_{(i)}^{T} \Delta z dS \right] ((\overline{T_{i}}^{n+1} - \overline{T_{i}}^{n}) / \Delta t)$$
(11)
$$\theta[L_{\overline{G},j}]^{n+1} + (1-\theta)[L_{\overline{G},j}]^{n+1} = -\sum_{i=N_{f}+1}^{N} \left[\int_{S_{c}} (\operatorname{grad} N_{(j)} h \boldsymbol{g} (\operatorname{grad} N_{(i)})^{T} \Delta z dS \right] (\theta \overline{T_{i}}^{n+1} + (1-\theta) \overline{T_{i}}^{n})$$

where we approximate the prescribed temperature rate rather than use its exact value.

2.4. *l*-adaptive error control

In order to control the error due to the surface approximation with collection of triangles, we adopt *l*-adaptive refinement method. The magnitude of the difference between the analytical distribution of temperature T(x), and an interpolation of this function on a finite element edge length $\Pi_l T(x)$, where *l* denotes mean edge length, is computed as

$$|T(x) - \Pi_l T(x)| \le C(\partial^2 T) l^2 \tag{12}$$

where $C(\partial^2 T)$ is rate of change whose magnitude depends on the curvatures of the function T in the immediate neighborhood of x. The errors of interpolation increase when the heat is changing faster (the higher the curvature of the function of the exact temperature T). The largest magnitude of the basis function gradient is produced by the smallest height in the triangle. The shortest height d_{\min} is estimated from the radius of the largest inscribed circle ρ , as $d_{\min} \approx O(\rho)$. This can be linked to the so-called shape quality of a triangle using the quality measure $\gamma = l/\rho$, as $d_{\min} \approx O(\gamma^{-1})l$. The magnitude of the basis function gradient is estimated as max grad $N_t(x) \approx \gamma/l$

$$|\operatorname{grad} T(x) - \operatorname{grad} \Pi_l T(x)| \le C(\partial^2 T)\gamma l \tag{13}$$

The errors of interpolation for the gradient of temperature increase with the increase of the curvature function of the exact temperature T, with the increase of the edge length, and the increase of the quality measure γ (i.e. the worse the shape of the triangle); Considering the curvatures at a fixed location as given, the error will decrease as O(l) as $l \rightarrow 0$ (note that this is one order lower than for the temperatures themselves: by reducing l with a factor of two, the error will decrease with the same factor). Importantly, from (13) we can read that the gradient is obtained by differentiation of the computed temperature, which immediately results in a reduction of the order of dependence on the mesh size. For quantity q, the error is then reduced by decreasing the edge length size

$$E_q(l) = q_{ex} - q_l \approx Cl^{\beta}$$

$$\lim_{l \to 0} E_q(l) = \lim_{l \to 0} Cl^{\beta} = 0 \quad \text{for } \beta > 0$$
(14)

where the exponent of the lenght size β is the rate of convergence.

3. Experimental results

The proposed method and all sparse techniques have been implemented in Matlab. All the experimental results are carried out on a PC with an Intel Core 2 Duo CPUs running at 2.66 GHz and with 3 GB of memory. To illustrate the proposed method, we consider a two-die stack consisting of 300 µm thick dies with a 10 mm by 10 mm cross-section. Heat sink and package thermal resistances are assumed to be 2 K/W and 20 K/W, respectively. These values are usually available from detailed thermal modeling of the heat sink and package. The interface resistance depends on the type of integration used. For example, the interface resistance is expected to be much lower for Cu-Cu bonding compared to *Cu-Sn-Cu* bonding. The effective thermal conductivity of the bond layer is a function of the area density of bond pads as well as the thermal conductivity of the filler material. For commonly used values of these parameters, the effective thermal conductivity of the bond layer falls in the same range as typical epoxies and dielectric materials. This happens despite the presence of highly conducting metal pads due to their low area density. While the thermal conductivity can be increased by increasing the bond pad density, this parameter is likely to be limited by electrical connection considerations. Thermal conductivity of silicon is taken to be 148 W/(mK) and that of copper interconnect 383 W/(mK). In comparison to the heat sink and package resistances, the silicon resistance is around 0.02 K/W. The substrate has 3 layers with thickness 3mm, 1mm, and 1mm from the bottom to the top. A wire with the size 1.5mm×3.5mm×0.6mm (Figure 4) is located at the coordinate of x=4mm, y=3mm, z=2mm. To illustrate in simulation plot only the temperature increment due to a device activity, the ambient temperature is assumed to be 0K. We assume that supply voltage is 1.2V and the current is 1mA. Temperature profile of I-form interconnect in Figure 5, computed within 2.1 seconds, shows that our solver can calculate temperature of multiple wires very accurately: output in our simulator ranges from 0.124K to 0.791K. Figure 6 shows temperature distribution of multilayer substrate at coordinates x=3mm, y=3mm, when high switching activity is recorded. The plot includes 19 timesteps, which cost approximately 33.5 seconds to represent the whole temperature distribution in the horizontal surface.

For comparison purposes, we implemented generalized finite element method, which can be found in several commercially available software packages (e.g. Hotspot [15], Ansys [16]). Figure 7 illustrates that the proposed Galerkin method with *l*-adaptive error control is 1~2 order of magnitude more accurate for comparable mesh size than corresponding generalized finite element method. For more complex circuit structures, additional increase has been observed. Furthermore, we compared modified Runge-Kutta solver with Euler (as in Hotspot [15]) and Newmark (in Ansys [16]). As shown in Table 1, the proposed method offers increased accuracy, while simultaneously increases solution efficiency.



Figure 4: Temperature distribution of I-form interconnect



Figure 5: Temperature profile of I-form interconnect at the (critical) - horizontal and vertical line crossing



Figure 6: Temperature distribution of three-layered substrate (zoomed-in version) with temperature conductivity of 1, 2, and 4 W/(mK) - top to bottom

Theoretically, proposed method can reach accuracy of $O(\Delta_t^4)$. On the other hand, the accuracy of Euler method is $O(\Delta_t^2)$. The errors in Euler scheme are dominated by the deterministic terms as long as the step-size is large enough.



Figure 7: Temperature error versus mesh size for the proposed (bold line) and generalized finite element method (dashed line) – I-form interconnect example

In more detail, the error of the method behaves like $O(\alpha^2 + \varepsilon \alpha + \varepsilon^2 \alpha^{1/2})$, when ε is used to measure the smallness of the temperature and α is the time-step. The smallness of the temperature also allows special estimates of the local error terms, which can be used to control the step-size. An efficient implementation of the Newmark methods for linear problems requires that direct methods (e.g. Gauss elimination) be used for the solution of the system of algebraic equations. When a step size should be updated, the prediction of the new step size has to be made such that the prescribed accuracy can be achieved with the least cost. The rate of convergence of the global error in the Newmark integration can be $O(\Delta_t^2)$. Correspondingly, the rate of convergence of the local error should achieve $O(\Delta_t^3)$. Suppose that the current time-step is α , then we have $O(\kappa \alpha^3)$, where κ is a constant depending on the exact solution.

4. Conclusions

Accurate temperature analysis is one of the foremost steps in the evaluation of successful high-performance 3D IC designs. This paper presents the thermal conduction model with surface boundary conditions and an efficient methodology for temperature analysis in 3D multi-layer substrate based on discontinuous Galerkin finite element method. As the results indicate, for comparable mesh size, the proposed method is 1~2 order of magnitude more accurate than corresponding, generalized finite element method.

Table 1: Accuracy comparison between Euler, Newmark

 and the proposed method at top surface

x-y[mm]	Euler [15]		Newmark [16]		This Paper	
	CPU	Err.%	CPU	Err.%	CPU	Err.%
1.17-3.42	1.76s	2.364	2.43s	0.375	2.04s	0.042
2.42-4.16	1.93s	2.147	2.54s	0.463	2.08s	0.028
3.86-4.28	1.86s	2.267	2.47s	0.428	2.29s	0.034
5.28-3.76	2.13s	2.325	2.63s	0.364	2.58s	0.041
6.68-4.54	1.87s	2.134	2.38s	0.448	2.86s	0.043
8.14-4.18	1.94s	2.246	2.45s	0.564	2.72s	0.037
9.64-3.86	1.98s	2.185	2.52s	0.474	2.47s	0.043

A. Zjajo, Thermal Analysis of 3D Integrated Circuits

5. References

- W. Topol, et al., "Three-dimensional integrated circuits", *IBM Journal of Research and Development*, vol. 50, no. 4/5, pp. 491-506, 2006.
- [2] C. Ababei, Y. Feng, B. Goplen, H. Mogal, T. P. Zhang, K. Bazargan, S. Sapatnekar, "Placement and routing in 3D integrated circuits", *IEEE Design and Test of Computers*, vol. 22, no. 6, pp. 520-531, 2005.
- [3] S. Im, K. Banerjee, "Full chip thermal analysis of planar (2-D) and vertically integrated (3-D) high performance ICs", *Proceedings of IEEE International Electron Devices Meeting*, pp. 727-730, 2000.
- [4] J. Torresola, C.-P. Chiu, G. Chrysler, D. Grannes, R. Mahajan, R. Prasher, A. Watwe, "Density factor approach to representing impact of die power maps on thermal management", *IEEE Transactions on Advanced Packaging*, vol. 28, no. 4, pp. 659-664, 2005.
- [5] J. Cong, J. Wei, Y. Zhang, "A thermal-driven floorplanning algorithm for 3D ICs", *Proceedings of International Conference on CAD*, pp. 306-313, 2004.
- [6] A.M. Ionescu, G. Reimbold, F. Mondon, "Current trends in the electrical characterization of low-k dielectrics", *Proceedings of IEEE International Semiconductor Conference*, pp. 27-36, 1999.
- [7] T.-Y. Chiang, S.J. Souri, C.O. Choi, K.C. Saraswat, "Thermal analysis of heterogeneous 3-D ICs with various integration schemes", *Proceedings of IEEE International Electron Devices Meeting*, pp. 681-684, 2001.
- [8] T.T. Wang, Y.M. Lee, C.C.P. Chen, "3D thermal ADI an efficient chip-level transient thermal simulator", *IEEE Transactions on CAD of Integrated Circuits and Systems*, vol. 21, no. 12, pp. 1434-1445, 2002.
- [9] K.J. Scott, "Electrostatic potential Green's functions for multi-layered dielectric media", *Philips Journal of Research*, vol. 45, pp. 293-324, 1990.
- [10] A. Vincenzi, A. Sridhar, M. Ruggiero, D. Atienze, "Fast thermal simulation of 2D/3D integrated circuits exploiting neural networks and GPUs", *Proceedings of IEEE International Symposium on Low Power Electronic Design*, pp. 151-156, 2011.
- [11] A.M. Niknejad, R. Gharpurey, R.G. Meyer, "Numerically stable Green function for modeling and analysis of substrate coupling in integrated circuits", *IEEE Transaction on CAD* of Integrated Circuits and Systems, vol. 17, no. 4, pp. 305-315, 1998.
- [12] B. Wang, P. Mazumder, "Fast thermal analysis for VLSI circuits via semi-analytical Green's function in multi-layer materials", *Proceedings of IEEE International Symposium* on Circuits and Systems, vol. 2, pp. 409-412, 2004.
- [13] N. Allec, Z. Hassan, L. Shang, R.P. Dick, R. Yang, "ThermalScope: Multi-scale thermal analysis for nanometerscale integrated circuits", *Proceedings of IEEE International Conference on Computer-Aided Design*, pp. 603-610, 2008.
- [14] L. Krivodonova, "Limiters for high-order discontinuous Galerkin methods", *Journal of Computational Physics*, no. 226, pp. 879-896, 2007.
- [15] K. Skadron, K. Sankaranarayanan, S. Velusamy, D. Tarjan, M.R. Stan, W. Huang, "Temperature-aware microarchitecture: modeling and implementation", ACM Transaction on Architecture Code Optimization, vol. 1, no. 1, pp. 94-125, 2004.
- [16] Ansys 10.0, http://www.ansys.com