CMOS SPAD Based on Photo-Carrier Diffusion Achieving PDP >40% From 440 to 580 nm at 4 V Excess Bias

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***Abstract*— A wide spectral response standard CMOS single-photon avalanche diode enabling simplified circuit interface for large array realization is reported. In this letter, the conventional p^+-nwell junction photon detection probability (PDP) profile is enhanced utilizing photo-carrier diffusion processes, resulting in a considerable expansion of the sensitivity spectrum of more than 30%. The proposed device achieves PDP greater than 40% from 440 to 580 nm at a low excess bias, while the dark count rate is 16 Hz/μm^2 and timing jitter (full-width at half-maximum) is 95 ps when using a 405-nm laser.**

***Index Terms*— Single-photon avalanche diode (SPAD), substrate isolation, low cross-talk, CMOS.**

I. Introduction

CMOS single-photon avalanche diode (SPAD) based imagers are being increasingly adopted in applications ranging from microscopy [1], [2] to biomedical diagnostics [3], [4] to space telescopes [5] to consumer electronics [6]. As the application field expands, the need to enhance SPAD performance, and especially spectral width, is also increasing. In CMOS technology, SPAD design is not only limited to the available implant/diffusion layers but it is also constrained by the need of circuit integration, so as to enable larger monolithic arrays. In this work we focus on realizing high performance CMOS SPADs that, at the same time, facilitate circuit integration.

In SPADs, spectral response can be theoretically enhanced either by designing the main junction with a wide depletion region or by widening the region where photo-carrier diffusion takes place. In case of wide depletion, an excess bias higher than 10V is required to enhance avalanche triggering probability [7]. In case of a widened of photo-carrier diffusion region, high sensitivity can be achieved with a relatively narrow depletion region and thus a lower excess bias. However, a drawback of the photo-carrier diffusion process is a long exponential tail in the time response of the SPAD [8]. CMOS SPADs [9], [10] designed using substrate as photon collection region have led to the realization of wide spectral sensitivity. However in [10], where the main junction was realized deeper in the substrate, has a large exponential tail resulting in a full-width at 10% of maximum jitter greater than 5ns for blue and 3ns for red sources. This timing performance is not acceptable in timing critical applications. Further, fill factor is generally low, even in advanced CMOS nodes, due to the need of an elaborated front-end circuitry, and cross-talk is high due to the lack of electrical isolation.

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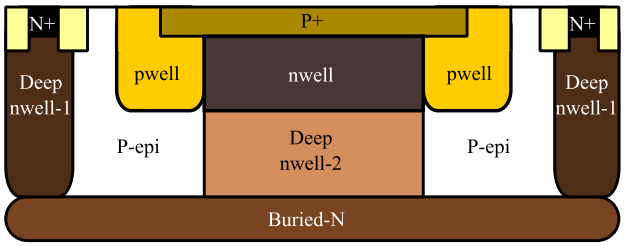

Fig. 1. SPAD cross-section design.

To ease circuit integration, in this work we report a substrate isolated SPAD, designed using narrower depletion junction with a relatively wider photon collection region. The SPAD fabricated in 180nm CMOS technology achieves PDP greater than 40% from 440nm to 580nm at 4V excess bias, whereas the DCR is 16 Hz/μm^2. To the best of our knowledge the achieved sensitivity is wider and higher than any other CMOS SPADs when operated at 4V excess bias, with comparable DCR. Lower DCR can be achieved but only in non-standard CMOS technologies, using a special enrichment implant [10]–[12], while the device presented in this work is designed in a standard CMOS technology. When compared to the SPADs designed using substrate as its photon collection region [10], the proposed design has better timing performance in the blue, and in the red it has relatively lower contribution towards the exponential tail.

The remainder of the letter is organized as follows: Section II describes the device design. Section III presents measurement results along with the state-of-the-art comparison. Section IV concludes the letter.

II. Device Design

The cross-section of the proposed SPAD designed using p+-nwell (NW) junction is presented in Fig. 1. Deep nwell-2 (DNW) and highly doped buried-N (BN) placed beneath nwell acts as a photon collection region. In this configuration, part of the photo-holes created in the quasi-neutral

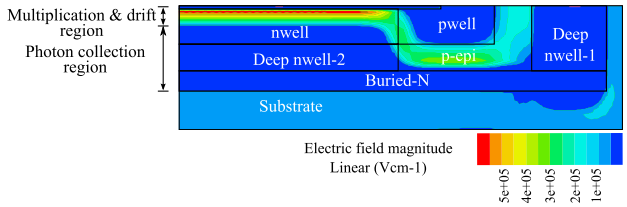

Fig. 2. Device electrical field simulation results preformed using MEDICI. The photon collection region including part of the nwell, DNW and BN is shown, along with multiplication and drift regions.

region of the BN, DNW and from the lower part of nwell could reach the multiplication region through the diffusion process. When compared to conventional p+-nwell devices [11]–[14], the proposed device has a wider photon collection region due to the BN layer protecting DNW from depletion, when the substrate junction is reverse biased.

Electric field simulation (Fig. 2) performed using MEDICI highlights the effectiveness of BN in protecting DNW from depletion, when the substrate junction is reverse biased. Further, the minimal depletion observed in BN due to its higher doping concentration suggests that almost the entirety of the BN volume, along with DNW, will function as a photon collection region. Note: the simulations were performed when the cathode was biased at the device breakdown, while the anode and the substrate were tied to ground. The technological parameters used in the simulations were provided to us by the foundry.

In this design the pwell, used as the guard ring, protects p+ edges from premature edge breakdown. Further, BN enabling substrate isolation, provides contact to DNW, while avoiding the need to counter-dope pwell, to result in improved guard ring effectiveness. For a circular device with a diameter of 12μm fabricated in 180nm CMOS technology, a breakdown voltage of 14.64V was measured.

III. Measurements

Measurements of the device of Fig. 1 were performed using an external active quench and recharge circuitry [7] that enables programmable dead time. For the experimental setup used in this work the minimum attainable dead time is 300ns [7].

Photon detection probability at various excess bias voltages is presented in Fig. 3.

Measurement results at 4V excess bias are compared with state-of-the-art CMOS SPADs [11]–[18] in Fig. 4. The proposed device surpasses state-of-the-art p+-NW junction based designs, mainly due to the presence of a wider photon collection region. When operating at 4V excess bias, the design presented here outperforms equivalent wide depletion devices designed using DNW [7]. Further, the reported PDP at 4V excess bias compares favorably with that of the state-of-the-art substrate isolated SPADs [7] operated at 10V excess bias.

When compared to SPADs [9], [10] designed using substrate as its photon collection region, it can be seen that the presented design has superior performance at 4V excess

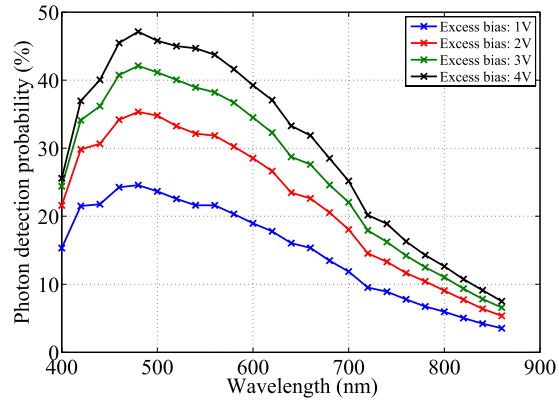

Fig. 3. Photo detection probability as a function of wavelength for different excess bias voltages.

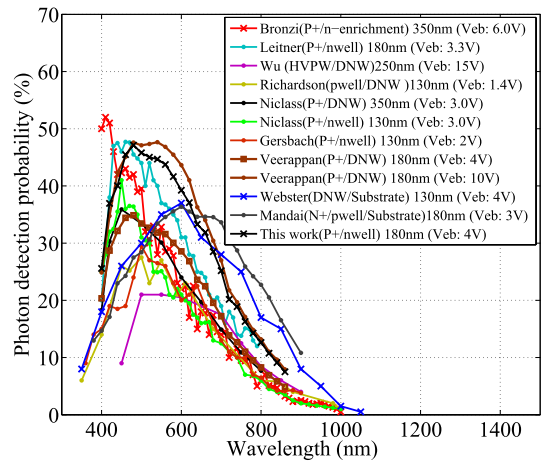

Fig. 4. State-of-the-art substrate isolated SPAD photo detection probability comparison.

bias up until 680nm. Higher sensitivity above 680nm in non-substrate isolated SPAD is due to the design allowing photo carrier collection from deep within the substrate through the diffusion process, where most of the lower energy photons are absorbed in silicon. In the design presented in this work the electric field resulting from reverse biasing the BN-substrate junction prevents photo-carriers generated in the substrate from reaching the multiplication region. Though the use of BN reduces the device sensitivity beyond 680nm, it helps in enabling substrate isolation and reducing the exponential tail of the time response of the device, when compared to non-substrate isolated SPADs.

Timing jitter measurements performed using red (637nm) and blue (405nm) lasers are presented in Fig. 5 a and b, respectively.

It can be seen that, when using a red laser, a relatively higher number of photons contribute to the exponential tail; suggesting that more red photons are collected through photo-carrier diffusion. This observation is in line with our design of the photon collection region, which is deeper into silicon, where most of the red photons are absorbed.

Jitter measurements showed a jitter of 141ps FWHM for red (637nm), and 95ps FWHM for blue (405nm) sources

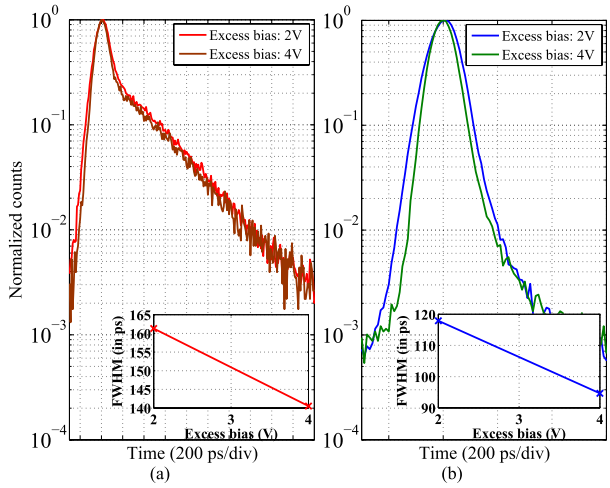

Fig. 5. Timing jitter measurement results when using (a) a red laser (637nm) (b) a blue laser (405nm).

TABLE I

STATE-OF-THE-ART JITTER COMPARISON WHEN USING BLUE LASER

	Blue full width at half maximum	Blue full width at 10% maximum
Webster 130nm	1.55ns(443nm)	>5ns
Mandai 180nm	182ps(405nm)	600ps(405nm)
Bronzi 350nm	85.8ps(390nm)	400ps(390nm)
Veerappan 180nm	70ps(405nm)	140ps(405nm)
This work 180nm	95ps(405nm)	180ps(405nm)

TABLE II

STATE-OF-THE-ART JITTER COMPARISON WHEN USING RED LASER

	Red full width at half maximum	Red full width at 10% maximum
Webster 130nm	77ps(654nm)	3ns(654nm)
Mandai 180nm	165ps(790nm)	550ps(790nm)
Bronzi 350nm	119ps(780nm)	-
Veerappan 180nm	86ps(637nm)	244ps(637nm)
This work 180nm	141ps(637nm)	690ps(637nm)

at 4V excess bias. When compared to [10], where the substrate was used as a photon collection region, the presented design has better timing performance in the blue and has lower contribution towards exponential tail in the red. Table I and II present the state-of-the-art CMOS SPAD jitter comparison when using blue and red laser sources. Along with generally reported full width at half maximum, full width at 10% maximum is also reported to include the exponential tail in jitter comparison. When compared to the state-of-the-art substrate isolated SPAD, it can be seen that the presented device has comparable timing performance when using blue sources, and for red sources, as expected, it has slightly worse full width at 10% maximum mainly due to presence of a diffusion tail, as discussed earlier.

Dark count rate (DCR) measurements were performed at 25 °C on four devices selected from different dies; the results are presented in Fig. 6. A DCR of 31 Hz at 1V excess bias was measured, and 1.8 kHz at 4V. Detailed DCR characterization performed at various temperatures is presented in Fig. 7. For this measurement, a device dead time of 10μs was chosen, to ensure negligible afterpulsing. The measurement highlights that the DCR dependence on voltage is higher than that on temperature, suggesting that a major contributor to noise is tunneling.

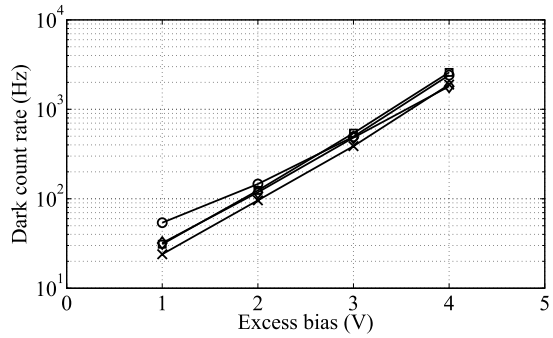

Fig. 6. Dark count rate measurement results from 4 different devices, when device dead time was set to 300ns.

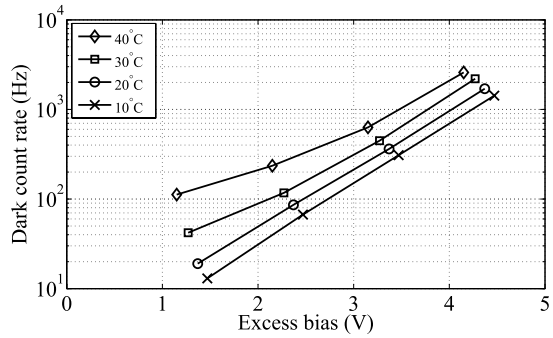

Fig. 7. Dark count rate measurement results at various temperatures.

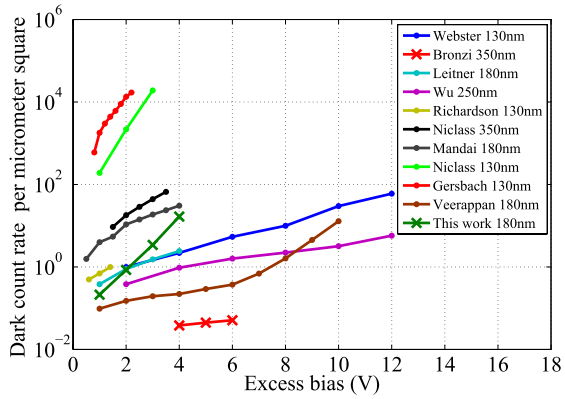

Fig. 8. State-of-the-art dark count rate comparison.

As can be seen in Fig. 8, the device presented in this work has slightly higher DCR than state-of-the-art substrate isolated devices [7], [15], [18] mainly due to tunneling. Low DCR SPADs presented in [11] use special enrichment implant, whereas the SPAD presented in this work was designed without any process modifications. Note: DCR is normalized in Fig. 8 and Fig. 9 to perform comparison with SPADs designed with different sizes.

Comparing device sensitivity (Fig. 4) to DCR (Fig. 8) at their operating excess bias, it can be seen that the proposed device is comparable to [7]. Further, the plot relating peak PDP to DCR of Fig. 9 corroborates the fact that the designed device performance is comparable to state-of-the-art substrate isolated wide spectral SPADs [7].

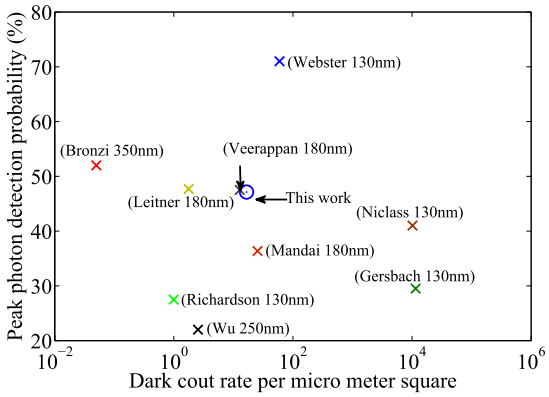

Fig. 9. State-of-the-art PDP to DCR comparison.

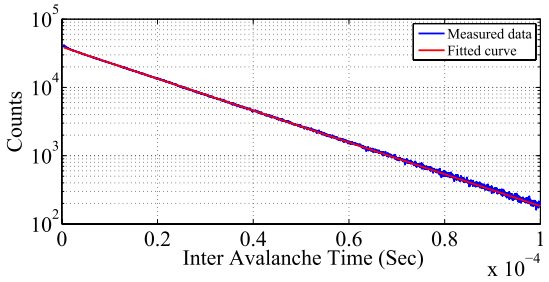

Fig. 10. Histogram of inter-avalanche SPAD firing at 4V excess bias, along with an exponential curve fitted to time larger than 2μs.

In the proposed devices, an afterpulsing probability of 0.2% was measured using inter-arrival avalanche histogramming at 4V excess bias. Measurement results presented in Fig. 10 suggests that the afterpulsing is negligible when the inter-avalanche time is more than 1.4μs. For this measurement a device dead time of 300ns was chosen.

IV. Conclusion

In this work, conventional p+-NW junction PDP is enhanced by increasing the photon collection region, thanks to the BN layer that suppresses depletion near DNW. The proposed device attains PDP >40% from 440nm to 580nm with merely 4V of excess bias. The achieved performance is comparable to state-of-the-art substrate-isolated SPADs operated at 10V of excess bias [7].

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References

[1] C. Veerappan *et al.*, "A 160×128 single-photon image sensor with on-pixel 55ps 10b time-to-digital converter," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2011, pp. 312–314.

[2] D. Tyndall, B. Rae, D. Li, J. Richardson, J. Arlt, and R. Henderson, "A 100mphoton/s time-resolved mini-silicon photomultiplier with on-chip fluorescence lifetime estimation in 0.13 μm CMOS imaging technology," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2012, pp. 122–124.

[3] L. H. C. Braga *et al.*, "An 8×16-pixel 92 kSPAD time-resolved sensor with on-pixel 64ps 12b TDC and 100 MS/s real-time energy histogramming in 0.13 μm CIS technology for PET/MRI applications," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2013, pp. 486–487.

[4] S. Mandai and E. Charbon, "Timing optimization of a H-tree based digital silicon photomultiplier," *J. Instrum.*, vol. 8, no. 9, p. 09016, Sep. 2013. [Online]. Available: http://stacks.iop.org/1748-0221/8/i=09/a=P09016

[5] Y. Maruyama, J. Blacksberg, and E. Charbon, "A 1024×8700ps time-gated SPAD line sensor for laser Raman spectroscopy and LIBS in space and rover-based planetary exploration," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2013, pp. 110–111.

[6] D. P. Baxter, "Proximity sensor having an array of single photon avalanche diodes and circuitry for switching off illumination source and associated method, computer readable medium and firmware," U.S. Patent 8 610 043, Dec. 17, 2013. [Online]. Available: http://www.google.com/patents/US8610043

[7] C. Veerappan and E. Charbon, "A substrate isolated CMOS SPAD enabling wide spectral response and low electrical crosstalk," *IEEE J. Sel. Topics Quantum Electron.*, vol. 20, no. 6, Nov./Dec. 2014, Art. ID 3801507.

[8] G. Ripamonti and S. Cova, "Carrier diffusion effects in the time-response of a fast photodiode," *Solid-State Electron.*, vol. 28, no. 9, pp. 925–931, Sep. 1985. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0038110185900863

[9] S. Mandai, M. W. Fishburn, Y. Maruyama, and E. Charbon, "A wide spectral range single-photon avalanche diode fabricated in an advanced 180 nm CMOS technology," *Opt. Exp.*, vol. 20, no. 6, pp. 5849–5857, Mar. 2012. [Online]. Available: http://www.opticsexpress.org/abstract.cfm?URI=oe-20-6-5849

[10] E. A. G. Webster, L. A. Grant, and R. K. Henderson, "A high-performance single-photon avalanche diode in 130-nm CMOS imaging technology," *IEEE Electron Device Lett.*, vol. 33, no. 11, pp. 1589–1591, Nov. 2012.

[11] D. Bronzi *et al.*, "Low-noise and large-area CMOS SPADs with timing response free from slow tails," in *Proc. Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2012, pp. 230–233.

[12] T. Leitner *et al.*, "Measurements and simulations of low dark count rate single photon avalanche diode device in a low voltage 180-nm CMOS image sensor technology," *IEEE Trans. Electron Devices*, vol. 60, no. 6, pp. 1982–1988, Jun. 2013.

[13] C. Niclass, M. Gersbach, R. Henderson, L. Grant, and E. Charbon, "A single photon avalanche diode implemented in 130-nm CMOS technology," *IEEE J. Sel. Topics Quantum Electron.*, vol. 13, no. 4, pp. 863–869, Jul./Aug. 2007.

[14] M. Gersbach, C. Niclass, E. Charbon, J. Richardson, R. Henderson, and L. Grant, "A single photon detector implemented in a 130 nm CMOS imaging process," in *Proc. 38th Eur. Solid-State Device Res. Conf. (ESSDERC)*, Sep. 2008, pp. 270–273.

[15] J.-Y. Wu, S.-C. Li, F.-Z. Hsu, and S.-D. Lin , "Two-dimensional mapping of photon counts in low-noise single-photon avalanche diodes," in *Proc. Int. Image Sensor Workshop (IISW)*, 2013, pp. 1–4.

[16] Z. Xiao, D. Pantic, and R. S. Popovic, "A new single photon avalanche diode in CMOS high-voltage technology," in *Proc. Int. Solid-State Sens. Actuators Microsyst. Conf. TRANSDUCERS*, Jun. 2007, pp. 1365–1368.

[17] C. L. Niclass, "Single-photon image sensors in CMOS: Picosecond resolution for three-dimensional imaging," Ph.D. dissertation, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, 2008.

[18] J. A. Richardson, L. A. Grant, and R. K. Henderson, "Low dark count single-photon avalanche diode structure compatible with standard nanometer scale CMOS technology," *IEEE Photon. Technol. Lett.*, vol. 21, no. 14, pp. 1020–1022, Jul. 15, 2009.