11.4 A 67,392-SPAD PVTB-Compensated Multi-Channel Digital SiPM with 432 Column-Parallel 48ps 17b TDCs for Endoscopic Time-of-Flight PET

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Positron emission tomography (PET) is a medical imaging technique for non-invasive detection of glucose metabolism in human organs, such as the brain, heart, and lungs. A positron-emitting molecule, generally Fluorodeoxyglucose-18 ("F-FDG), is injected and subsequently identified by coincident detection of two gamma photons released during the annihilation of an electron with the positron lost by ¹⁶F-FDG. Conventionally, coincident gamma photons are detected through scintillation by two sensors placed at 180° in a ring of identical sensors (Fig. 11.4.1a). In EndoTOFPET-US [1], two sensors are used, one placed in a semicircular ring outside the patient and the other placed on an endoscope (Fig. 11.4.1b). The endoscopic sensor is a miniaturized array of silicon photomultipliers (SiPMs) coupled to a mini-scintillator. To exploit the Fishburn-Seifert lower bound [2] in timing resolution, a large number of photon timestamps must be generated, as is done in a multi-channel digital SiPM (MD-SiPM).

In this paper, an endoscopic sensor is described, to detect 67,392 photons and the first 432 time-of-arrival events in every detection frame of 6.4 μ s. The sensor comprises 9×18 MD-SiPMs, a high-voltage generator, and a bank of 432 column-parallel time-to-digital converters (TDCs). Figure 11.4.2 shows the block diagram of the endoscopic sensor chip. Each MD-SiPM can capture up to 48 timestamps in a frame; it comprises 416 cells that detect scintillation photons, so as to provide an estimate of the gamma photon energy, which is proportional to the number of photons emitted. A mechanism called 'smart reset' is used to filter spurious events that have insufficient or excessive energy. The algorithm is shown in the bottom inset of Fig. 11.4.2. Upon detection of a candidate gamma event, its energy is estimated in the 'Energy Calculator', which scans all MD-SiPMs with the highest number of fired cells, reading out up to 4 energy contents per frame.

The cell's core is a single-photon avalanche diode (SPAD). A SPAD, implemented as shared cathode p+/deep n-well junction, is a photodiode biased above breakdown by excess bias Ve, to operate in Geiger mode. A detected photon may trigger an avalanche that is quenched by a large impedance at the anode. When MASKDATA is 'high' and MASK is asserted, a static memory is set, thus enabling (or unmasking) the SPAD through the AND. In this mode, the SPAD anode can be grounded by briefly asserting 'RST', thus recharging the SPAD. A 1b counter, implemented as static memory, records the photon detection for energy calculation; it is read out via the 'ENERGY' line. A direct connection to a pull-down transistor, enabled by assertion of 'ROWCALSEL', transfers the pulse generated upon photon detection to the 'TIMING' line.

Ve determines the sensitivity of a SPAD, or photon detection probability (PDP), provided that the breakdown voltage ($|V_{BD}|$) is constant. In reality, $|V_{BD}|$ varies as a function of process variations and temperature, thus the operating voltage (V_{OP} =| $V_{BD}|$ +Ve) must be adjusted to keep Ve constant. This function is implemented by a digitally controlled charge pump (DCP) that continuously monitors Ve and adjusts the output voltage so as to keep Ve unchanged, irrespective of MD-SiPM activity due to variable light *brightness*, therefore the PVTB denomination. The DCP, based on [3], resembles an 11-stage Dickson architecture, except for a parasitic capacitance in each stage that can be digitally modulated via NMOS switches. The input voltage of the DCP is VIN=3.3 V, the nominal power supply; the circuit is converted to a digital code, which in turn generates an update for the DCP in a closed loop, where dark count rate (DCR) is used to estimate the temperature.

There are 9 columns of 18 MD-SiPMs each of which shares 48 TDCs; each 'TIMING' line driving a TDC is buffered, so as to minimize skews due to different signal propagation. There is a matrix of 48×9 TDCs in the chip controlled by a global VCO that generates four phases (ϕ_0 through ϕ_3), as shown in Fig. 11.4.3. The VCO is stabilized by a bandgap reference to a programmable frequency

centered at 644MHz. The TDC lines ('Start₁' through 'Start₄₃₂') drive an array of dual phase detectors that enable interpolation into 32 phases for a 5b resolution (fine), thus providing a PVT controlled LSB value of 48.5ps. A 12b counter provides the coarse resolution, to achieve a total of 17b. Thanks to this centralized architecture, this design vastly improves upon [4] by minimizing skew across the TDC matrix and revealing a worst-case crosstalk of 1.8%.

Figure 11.4.4 shows the timing diagram of the smart reset mechanism. A global reset (GRST) resets all the cells and TDCs for 12.5ns (0.5 clock cycle). After a programmable time of 50 to 200ns, noise may have occurred, temporarily occupying a number of TDCs (in this example: 2). If the count of these noise events does not exceed a given threshold (in this example: 4), then all fired TDCs are reset via SRST. If the count exceeds the threshold, then no reset is performed, thus achieving a count proportional to the energy of the gamma ray that hit the scintillator. The content of the array is eventually read out at the end of the frame. The insets show an actual measurement with and without smart reset, as well as the TDC occupancy statistics within 3µs.

Figure 11.4.5 shows the energy spectrum of gamma photons emitted by the annihilation of an electron and a positron released by a ²²Na source. During the measurement, the sensor was coupled with a 3×3×10mm³ LYSO scintillator; the spectrum has a peak at 511keV. Compton events and the peak at 1275keV emitted by ²²Na make up for the remainder of the spectrum. The energy resolution, a measure of the efficacy of a filter to eliminate non-511keV photons is 15.7% (FWHM). The top inset shows a normalized space density map of the photons generated during gamma scintillation. The right inset shows the sensor response to a 405nm commercial laser source (ALDS GmBH, Germany) mimicking scintillation. The measured single-photon timing resolution (SPTR) is 327ps (FWHM).

Figure 11.4.6 summarizes the performance of the chip and compares it with the state of the art. The sensor has one of the highest levels of integration to date, and the highest number of TDCs on chip and per SiPM. The power consumption per TDC is the lowest for any SiPM. The SPAD pixel has negligible optical crosstalk and afterpulsing at 3μ s. The chip micrograph is shown in Fig. 11.4.7. The figure also shows a close-up of the MD-SiPM and of the cell it is based on in an inset. Also visible in the figure are the high voltage generator and the other components highlighted in the picture: column-parallel TDCs, smart reset detection logic, energy calculator, and masking mechanism. The chip, fabricated in a 0.35 μ m HV CMOS technology, has a total area of 19.9×7.6mm².

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Figure 11.4.3: Block and timing diagram of the TDCs. A ring oscillator distributes 8 phases to 432 dual phase detectors, shown in the inset. The TDCs operate from the start of each channel, Start_j, to the global stop that controls signal EN, while RST resets all TDCs.



Figure 11.4.5: Energy spectrum measured by the sensor when coupled with a 3×3×10mm³ LYSO scintillator and exposed to a ²²Na source (150µCi). Normalized photon space density map generated by scintillation (top inset). Response to a 405nm 40ps FWHM laser pulse (right inset). Figure 11.4.4: Smart reset: timing diagram for a full frame. The left inset shows an actual case whereby TH_{tdc} was set to 35 at 1.44, 1.76, and 1.92µs, respectively. The right inset shows the TDC occupancy statistics with and without smart reset.

	Parameter	This Work	Mandai et al. [4]	Frach et al. [6]	Braga et al. [5]
Sensor	Technology	HV CMOS 0.35µm	HV CMOS 0.35µm	Non-standard 0.18µm	CIS 0.13µm
	# SiPMs	9 × 18	4 × 4	1 (4)	8 × 16
	# SPAD / SIPM	416	416	6,400 (3,200†)	720
	Sensor area (mm ²)	19.9 × 7.6	5.24 × 4.22	7.8 × 7.2	9.85 × 5.45
	Clock (MHz)	40	40	Not reported	100
	Power (mW)	990 (all TDCs on)	330	Not reported	120
TDC	# TDCs / SiPM col.	48	48	2	1
	Total # TDCs	432	192	2 (8†)	128
	Power / TDC (µA)	500	570	Not reported	948
	TDC LSB (ps)	48.5	44	24	64.5
	TDC DNL/INL (LSB)	±0.75 / +42.1	2/3.5	Not reported	±0.26 / +2.33.9
SiPM	Cell pitch (µm × µm)	30 × 50	30 × 50	59 × 32 (59 × 64†)	16.27
	Total DCR (Mcps)	15 (20C, 20% mask)	10 (20C, 20% mask)	~2 (20C, 5% mask)	30.3 (20C, 0% mask)
	Fill factor (%)	57	55.6	50 (78†)	43
	SPTR (ps FWHM, λ=420nm)	327 @ λ=405nm, Ve=3.0V	179 @ Ve=3.0V	> 350 (60†) @ λ=410nm	239 @ λ=470nm
	Optical crosstalk (%)	<1.8	<10	18† @ Ve=3.3V	Not reported
	SiPM area	800 × 800µm ²	800 × 800µm ²	3.8 × 3.3mm ²	610 × 571µm ²
High Voltage Generator	VOP range (V)	21.4 – 25	No Integrated High Voltage Generator † : Improved data, as presented in later papers/talks.		
	Temperature range (°C)	0 – 70			
	Load range (µA)	0 – 1400			
	Max. Ve drift (V)	2.92 - 3.09			
	Max. Ve droop (V)	2.98 - 3.10			
SPAD	PDE at 420nm (%)	18.6 @ Ve=3.5V	17	15 (35†)	12† @ Ve=1.5V
	Median DCR (cps/µm ² , 20C)	43 @ Ve=3.5V	39 @ Ve=3.0V	0.19	64† @ Ve=1.5V
	Jitter (ps)	104 @ λ=405nm, Ve=3.0V	114 @ λ=405nm	124 @ λ=410nm	150 @ Ve=1.4V

Figure 11.4.6: Performance summary for the sensor chip in comparison with the literature.

