

A Low-Power Low-Voltage High-Performance Fully Differential OTA in 65-nm CMOS Process

Mingxin Song, Jinghua Yin, Yijiang Cao, Zhao Jin
 Dept. of the Electrical Science and Technology
 Harbin University of Science and Technology
 Harbin, China
 yinjinghua1@126.com

Amir Zjajo
 The Circuit and Systems Group
 Delft University of Technology
 Delft, The Netherlands
 amir.zjajo@ieee.org

Abstract—This paper presents the design and analysis of high speed, high gain and fully differential operational transconductance amplifier (OTA) implemented in 65-nm digital CMOS process. The OTA, which employ a folded-cascode topology with gain boosting technique, has rail-to-rail input swing and large output swing. The result shows the DC gain of 82 dB and a unity-gain frequency of 477MHz with phase margin of 59° (double 1-pF load) while consuming 4.8 mW. For the normal corner, the settling time to < 0.05% accuracy is 10 ns.

Keywords- CMOS integrated circuits; OTA; gain-boosting

I. INTRODUCTION

As the channel lengths of MOSFET keep shrinking, the transistors are becoming faster and power efficient. On the other hand, accompanied low supply voltage and the short channel effects such as Early voltage reduce the gain of a simple transistor stage making the realization of high-gain, wide-input and -output voltage range amplifiers for high performance analog circuits in deep-sub-um technology very challenging task. Speed and accuracy are two of the most important properties of amplifiers in analog circuits such as A/D converters, switched capacitor filter and sample-and-hold amplifiers [1-3]. The settling speed mainly depends on the unity-gain frequency and a single pole settling time while high settling accuracy is due to high DC gain of the op-amp circuits. However, optimizing amplifiers for speed and gain usually leads to contradictory demand. The high-gain requirement leads to multistage designs with long-channel devices biased at low current levels, whereas the high-speed requirement calls for a single stage design with short channel devices biased at high current levels. One technique, which helps to increase the op-amp DC gain without sacrificing the unity-gain frequency, is the gain-boosting technique introduced in [4] and firstly applied to the folded cascode op-amp in [5]. The proper design procedure of gain boosting cascode amplifier has been a subject of study during the past years [6-8]. In [6], a DC gain of 95 dB and a gain bandwidth (GBW) of 412MHz is attained, while consuming 12.8mW. In [7], a DC gain of 106 dB 57MHz GBW was realized. A complex three-stage structure in [8] achieves 84dB DC gain and GBW of 200MHz while consuming 10mW. In this paper, we present fully differential op-amp with 82 dB DC gain and 477MHz unity gain frequency, while consuming only 4.8 mW.

II. BASIC PRINCIPLE OF GAIN-BOOSTING

As shown in Fig. 1 the basic idea of gain boosting is based on negative feedback loop to set the drain voltage of transistor M2. The output impedance of the circuit is increased by the gain of the additional gain stage, A_{aux} :

$$R_{out} = (g_{m2}r_{o2}(A_{aux} + 1) + 1)r_{o1} + r_{o2} \approx g_{m2}r_{o2}A_{aux}r_{o1} \quad (1)$$

This increased output resistance results in several orders of improvements on the overall gain.

$$A_{tot} = g_{m1}R_{out} = A_{orig}A_{aux} \quad (2)$$

For reason concerning stability and fast settling, the safe range for the unity-gain frequency of the additional amplifier $\omega_{\mu,a}$ is limited within

$$\beta\omega_{\mu,m} \leq \omega_{u,a} \leq \omega_{2p,m} \quad (3)$$

$$\beta = \frac{C_{fb}}{C_{in} + C_{inpar} + C_{fb}} \quad (4)$$

Where $\beta\omega_{\mu,m}$ is the closed-loop dominant pole frequency, $\omega_{\mu,m}$ denotes the open-loop unity-gain frequency of the main amplifier and β is the closed loop with feedback factor (the fraction of the op-amp output voltage that is fed back to the op-amp input) defined through opamp's input capacitance C_{in} , parasitic capacitance C_{inpar} and feedback capacitance C_{fb} .

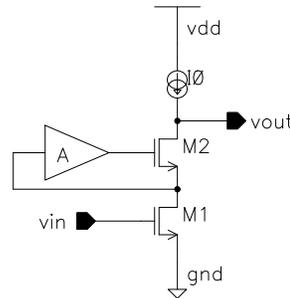


Figure 1. Cascode gain stage with gain enhancement

Typical gain-boost structures are shown in Fig.2. Folded-cascode architecture with gain-boosting is usually chosen as the optimum structure for the applications in a low supply voltage. It offers relatively larger output swing and better single-pole roll-off frequency response than non-folded-cascode

architecture with gain-boosting. The additional amplifier has two versions: the single-ended architecture and the fully differential architecture. The single-ended version of the boosters has some undesired effects, such as having an extra pole from an internal current mirror and noise generated by the biasing circuit. On the other hand, fully differential amplifier requires common-mode feedback (CMFB) circuit.

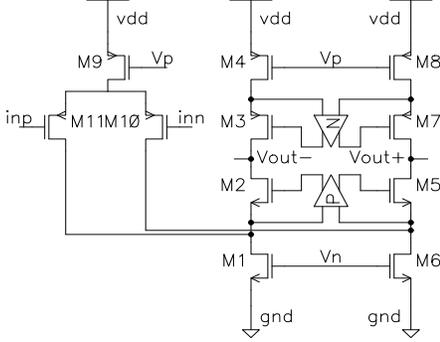


Figure 2. Folded-cascode architecture with fully differential booster

III. CIRCUITS DESIGN AND ANALYSIS

A. Specification

The total relative settling error ε is sum of both the static error ε_s and dynamic error ε_d contributions

$$\varepsilon = \varepsilon_s + \varepsilon_d \quad (5)$$

Considering the amplifier used in a charge-transfer SC circuit, ε_s resulting from a limited DC gain, A , is obtained as:

$$\varepsilon_s = \frac{1}{\beta A} \quad (6)$$

In this case, ε_s should be less than 0.2% while the factor β is 0.5. This means the gain must achieve at least 60dB.

$$\varepsilon_d = e^{-\frac{\tau}{\tau}} \quad (7)$$

$$\tau = \frac{1}{\beta \cdot G B W} \quad (8)$$

At the same time, the amplifier should have a settling time of less than 10ns to achieve 0.1%. Thus, the linear settling time T is equal to 8τ leading to the OTA gain-bandwidth of at least 120MHz. However, considering the slew time, t_{slew} (in this case, t_{slew} is about 3τ), GBW of OTA should be larger than 170 MHz.

$$t_{slew} = \tau \left(\frac{\gamma |V_{step}|}{\sqrt{2} V_{on}} - 1 \right) \quad (9)$$

$$\lambda = \frac{C_{in}}{C_{in} + C_{inpar} + \frac{C_{fb}(C_L + C_{outpar})}{C_{fb} + C_L + C_{outpar}}} \quad (10)$$

Where V_{on} is the overdriven voltage of the input MOS pair and V_{step} is the instantaneous value of V_{in} . Taking into account parasitical capacitance, the effective capacitance is about 2pF.

$$G B W = \frac{g_m}{C_{Leff}} \quad (11)$$

$$C_{Leff} = C_L + C_{outpar} + \beta(C_{in} + C_{inpar}) \quad (12)$$

B. The main amplifier

The input voltage of gain-boosting structures with p-channel input pair shown in Fig. 3 is limited in a range given by Eq. 13. Similarly, for the one with n-channel input pair, the input voltage is limited in a range given by Eq. 14.

$$V_{SS} \leq V_{in} \leq (V_{DD} - |V_{Dsat}| - |V_{Tp}|) \quad (13)$$

$$(V_{SS} + V_{Dsat} + V_{Tp}) \leq V_{in} \leq V_{DD} \quad (14)$$

The unavailable range of the input voltage is about half of the supply voltage, which is unacceptable for the low voltage application. In a conventional compact op-amp with rail-to-rail input stage^[9] an n -channel input pair T_{1-2} is placed in parallel with a p -channel input pair T_{3-4} to process signals from rail to rail. To make the transconductance as a function of the common-mode input voltage constant a simple feed-forward method is applying current switches T_{5-8} . The current switches^[10] are divided into two transistors of which the drains are connected to the drains of the corresponding input-stage transistors. By adding the currents to the outputs of the input-stage transistors the output current of the input stage does not change as a function of the common-mode input voltage. Since relatively small current-switch transistors can be used, their noise contribution to the noise of the amplifier can be made relatively small.

The transistors of the output stage have three constrains: the sum of the saturation voltage for the transistors in one of the output branches must fit into the voltage headroom, resulting as the difference between the voltage supply and the desired output voltage swing. Second, the transconductance of the cascading transistors T_{17-20} must be high enough, in order to boost the output resistance of the cascode, allowing a high enough dc gain. Finally the saturation voltage of the active loads T_{15-16} and T_{21-22} must be maximized, in order to reduce the extra noise contribution of the output stage. These considerations underline a tradeoff between fitting the saturation voltage into the voltage headroom and minimizing the noise contribution. A good compromise is to make the cascading transistors larger than the active loads: in such a way the transconductance of the cascading transistors is maximized, boosting the dc gain, while their saturation voltage is reduced, allowing for a larger saturation voltage for the active loads, without exceeding the voltage headroom.

C. Auxiliary Amplifier

The auxiliary gain-boosting amplifiers are implemented with folded cascode op-amps with fully differential output with an n -channel and p -channel differential pair employed in the top and bottom auxiliary amplifier, respectively. The source-gate capacitances of T_{17-20} now form Miller capacitance, which are connected between the inputs and outputs of the additional amps. Now, the capacitances seen at the folded node are boosted from C_{gs} to $(1+A_{aux})C_{gs}$, where A_{aux} is the gain of the auxiliary amplifiers reducing the second pole frequency ω_{p2} and thus degrading the phase margin of the op-amp.

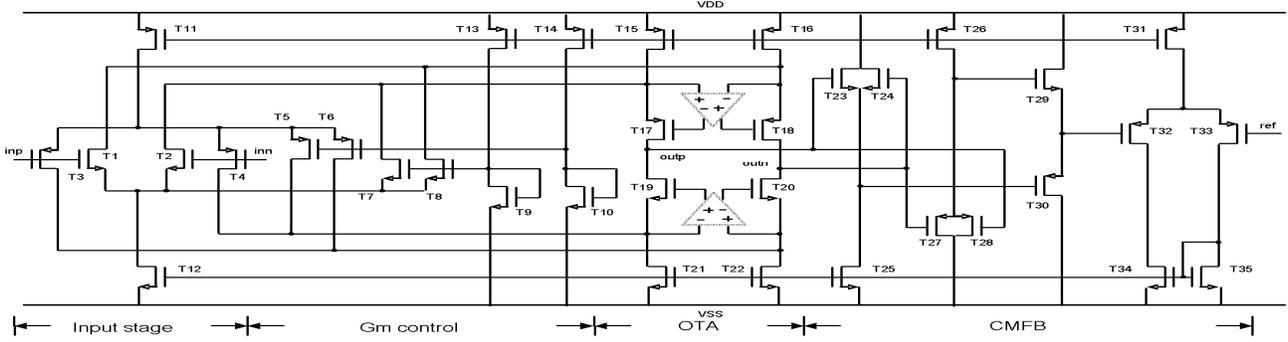


Figure 3. The proposed op-amp with CMFB circuit

In high-speed designs with deep feedback the second pole frequency ω_{p2} is often not much higher than the first pole frequency ω_{p1} making the gain-bandwidth product optimization complicated. In order to track process variation and increase the dominant pole frequency of the auxiliary amplifier, the extra capacitors, C_C , (not shown in Fig. 3), are added at the outputs of auxiliary amplifiers to fine-tune ω_{aux} [11]. However, it needs to be pointed out that the final results should be insensitive to the value of C_C , which is an essential part of the verification process.

D. Biasing circuit

In order to achieve large output swing, the high-swing cascode biasing circuits is adopted. Power dissipation in biasing is small since the current through biasing network is 10 times smaller than that through main amplifier.

E. CMFB circuits

Currently, common-mode feedback circuits are generally realized by either circuits based on differential-differential amplifier (DDA) or switched capacitor (SC) structures. However, CMFB based on SC circuits is not preferable for continuous-time systems or high-frequency application. CMFBs based on symmetrical and asymmetrical DDA [12-13] are not suitable for systems with large output signal swing (especially in low supply voltage). In contrast, balanced resistor/capacitor DDA [14] can operate with large output swing, although it is not appropriate for high output impedance system or the circuits fabricated in deep-submicron technologies. A common-mode feedback circuit comprising of T_{23-35} [15], where the resistor/capacitor network in balanced resistor/capacitor differential-difference amplifier common-mode feedback structure is replaced by a transistor network consisting of T_{23-28} , so that the output common mode level can be sensed without changing the impedance at the system output. The signal path from the opamp output to the gate of T_{32} is built exclusively by source-follower stages, so the gate voltage $V_{G(T32)}$ is a monotonically increasing function of the output common-mode level. Similarly, since T_{23-28} are complementary types of transistors, the output common-mode level is guaranteed to be detected in full-swing range without pulling any transistors of T_{31-35} away from the saturation region. Additionally, since all nodes in the network T_{23-28} are low impedance nodes, no additional stability problems will

occur. Compared with other common-mode feedback circuits, this implementation provides the widest linear input range, smallest output common-mode level error, largest output swing and has no interference to the op-amp output impedance.

IV. RESULTS

The operations and performances of deep-submicron integrated circuits are affected significantly by the variations of process parameters, power supply voltages and operating temperatures. Circuit simulation for all the combinations of process-voltage-temperature (PVT) conditions, known as PVT simulation, is emerging as a must for analog and RF circuit. Simulation studies for all 5 process-corners (SS, SF, TT, FF, FS) and 3 different temperatures (0°, 27°, 75°C) under 1.05V, 1.2V, 1.35 supply voltages were conducted.

Tab.I summarizes the performance of OTA in the different process corners over a wide temperature range and the different supply voltages. This clearly demonstrates this design.

TABLE I. SUMMARY OF SIMULATION RESULTS

| Corner VDD(V)/T(°C) | DC gain (dB) | GBW (MHz) | Phase (°) |
|------------------------|-----------------|--------------|--------------|
| 1.05/0 | 78.9 | 483 | 61.7 |
| 1.05/27 | 78.6 | 480 | 61.3 |
| 1.05/75 | 76.7 | 457 | 60.0 |
| 1.2/0 | 81.8 | 473 | 58.3 |
| 1.2/27 | 82.1 | 477 | 58.7 |
| 1.2/75 | 81.9 | 463 | 58.5 |
| 1.35/0 | 77.7 | 439 | 55.6 |
| 1.35/27 | 78.9 | 455 | 56.2 |
| 1.35/75 | 79.7 | 455 | 56.8 |

Fig.4 shows the range of input voltage when simulating with normal process and four process corner. As can be seen, for all corners, the gains of the OTA are the constants from VSS to VDD. In typical situations, DC gains of 82 dB were achieved with rail-to-rail input voltage. Furthermore, simulation results from an AC analysis showed GBW over 400MHz and nearly 60° phase-margin with 1pF load (Fig.5). The total power consumption of the amplifier was about 4.8mW.

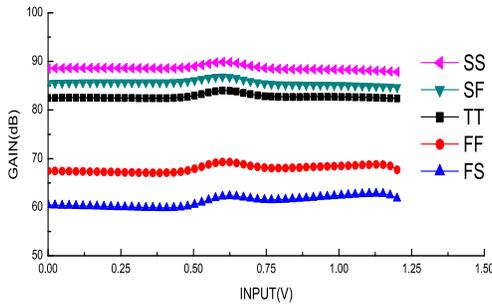


Figure 4. The plot of the gains vs input voltage

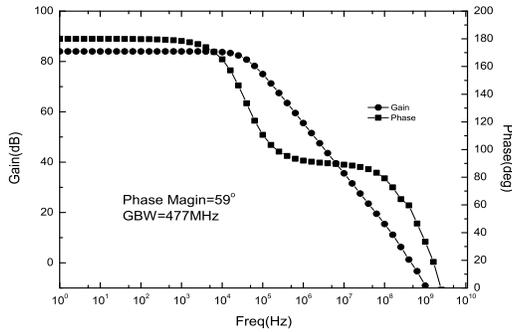


Figure 5. Bode plots

The settling behavior of the OTA is simulated in a closed-loop configuration. Fig.6 indicates gain-boosting amplifier settling performance. The transient simulation shows the OTA settles to the final value in 0.05% accuracy of 0.4-V step within 10ns in the normal corner, 0.5% for the worst corner and 0.03% for the best corner.

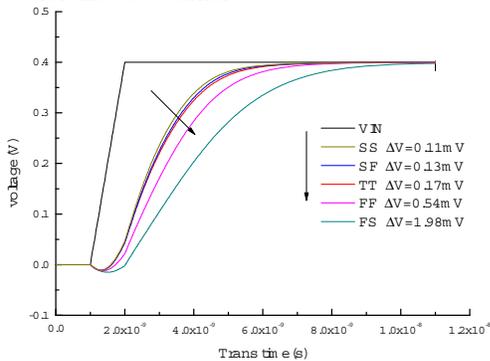


Figure 6. OTA step response

In Tab.II, comparing this OTA with other works, it's the high bandwidth at low power make it a proper choice for high-frequency application.

TABLE II. PERFORMANCE COMPARISON

| Reference | Ref. [6] | Ref. [7] | Ref. [8] | This work |
|-------------|----------|----------|----------|-----------|
| Process(nm) | 350 | 120 | 65 | 65 |
| VDD(V) | 3 | 1.2 | 1 | 1.2 |
| DC gain(dB) | 95 | 106 | 84 | 82 |
| GBW(MHz) | 412 | 57 | 200 | 477 |
| Phase(°) | 75 | 71 | 76 | 60 |
| CL(pF) | 1.9 | 5.5 | 1 | 1 |
| Power(mW) | 12.8 | 2.42 | 10.17 | 4.8 |

V. CONCLUSION

An op-amp in 65nm CMOS with a rail-to-rail input stage with the bandwidth of 477 MHz at a supply voltage of 1.2V is described. At the same time, a gain exceeding 80dB and a phase margin of 60 degree are achieved for loads of 1 pF in the normal corner. Its high gain and wide bandwidth make it a proper choice for wireless communications and other high-frequency application. This work will be employed in the programmable analog sinewave generator design.

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