A 1.2V 55mW 12bits Self-Calibrated Dual-Residue Analog to Digital Converter in 90 nm CMOS

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***Abstract*—This paper reports design, optimization, efficiency and measurement results of the 12 bits dual-residue multi-step A/D converter. The calibration procedure based on the steepest-descent estimation method is enhanced with dedicated embedded sensors, which register on-chip process parameter and temperature variations. The prototype A/D converter with performance of 68.6 dB SNDR, 70.3 dB SNR, 78.1 dB SFDR, 11.1 ENOB at 60 MS/s has been fabricated in standard single poly, six metal 90 nm CMOS, consumes only 55 mW and measures 0.75 mm^2. The on-chip calibration logic occupies an area of 0.14 mm^2 and consumes 11 mW of power.**

Keywords-analog to digital converter, dual residue technique, calibration, process variation monitoring

I. INTRODUCTION

The static parameters of a multi-step analog to digital (A/D) converter are determined by analog errors in various A/D converter components. Therefore, a major challenge in A/D converter calibration is to estimate the contribution of those individual errors to the overall A/D converter linearity parameters. The observation of important design and technology parameters, such as temperature, threshold voltage, etc., is enhanced with dedicated sensors embedded within the functional cores [1]. The steps causing discontinuities in the A/D converter's stage transfer functions can be analyzed, minimized or corrected with a wide variety of calibration techniques [2]-[7]. The mismatch and error attached to each step can either be averaged out, or their magnitude can be measured and corrected. In general, most calibration methods require that a reference signal is available in the digital domain, this being the signal that the actual stage output of the A/D converter is compared with. This reference signal is in the ideal case a perfect, infinite resolution, sampled version of the signal applied to the A/D converter under test. Nevertheless, in a practical situation, the reference signal must be estimated in some way. This can be accomplished by incorporating auxiliary devices such as a reference A/D converter, sampling the same signal as the A/D converter under test [8], or a D/A converter feeding a digitally generated signal to the A/D converter under test [9].

In this paper, such an A/D converter is augmented with dedicated sensors embedded within the converter to supplement the circuit calibration and to guide the verification process with the information obtained through the monitoring process. Furthermore, the design-for-test (DfT) capabilities permit a multi-step A/D converter re-configuration in such a way that all sub-blocks are tested for their full input range allowing full functional observability and controllability. Additionally, in the proposed method the overlap between the conversion ranges of two stages is considered to avoid conflicting operational situations that can either mask faults or give an incorrect interpretation.

II. CONCEPT OF PROCESS VARIATION MONITORING ENHANCED CALIBRATION

Even though extensive research [10]-[13] has been done to estimate the various errors in different A/D converter architectures, the use of DfT and dedicated sensors for the analysis of multi-step A/D converters to update parameter estimates has been negligible. The influence of the architecture on A/D converter modeling is investigated in [10]. In [11] with the use of some additional sensor circuitry, pipeline A/D converters are evaluated in terms of their response to substrate noises globally existing in a chip. In [12], the differential nonlinearity test data is employed for fault location and identification of the analog components in the flash A/D converter, and in [13] it is shown how a given calibration data set may be used to extract estimates of a specific error performance. Functional faults in each of the analog components in a multi-step A/D converter affect the transfer function differently [11], and analyzing this property forms the basis of our approach. The A/D converter characteristics may also change while it is used, e.g. due to temperature change and component aging. This means that the A/D converter has to be reevaluated at regular intervals through temperature sensors to examine its performance. Each stage of the A/D converter under test is evaluated experimentally, i.e. a signal is fed to the input of each stage of the A/D converter and the transfer characteristics of each stage of the A/D converter is determined from the outcome.

A. A/D Converter Architecture

The overall multi-step A/D converter consists primarily of non-critical low-power components, such as low-resolution quantizers, switches and open-loop amplifiers. As shown in Figure 1, the input signal is sampled by a three-time interleaved sample-and-hold (S/H), which eliminates the need for re-sampling of the signal after each quantization stage. The resulting sampled signal is then further processed in three steps, namely, the coarse (4 bit), the mid (4 bit) and the fine (6 bit) steps. The acquired signal from the coarse quantization is stored in a latch and is also applied to a switch unit to select the references for the mid quantization in the next clock phase. The selected reference signals are combined with the held input signals from the S/H in two mid residue amplifiers. Similarly,

the outputs of both coarse and mid A/D converters are combined together in order to select proper references for the fine quantization. Correspondingly, these references are combined with the sampled input signal in two fine residue amplifiers, before they are processed in a fine stage. Typically, the full range of the mid quantization resistance ladder is longer than one step in the coarse quantization ladder. With this over-range compensation in the mid ladder (e.g. similar principle is applicable to the fine ladder as well) the static errors can be corrected since the signal still lies in the range of the mid ladder. This means that the output of the A/D converter is redundant and it is not possible, from the digital output, to find the values from each sub-ranging step without employing dedicated DfT [14].

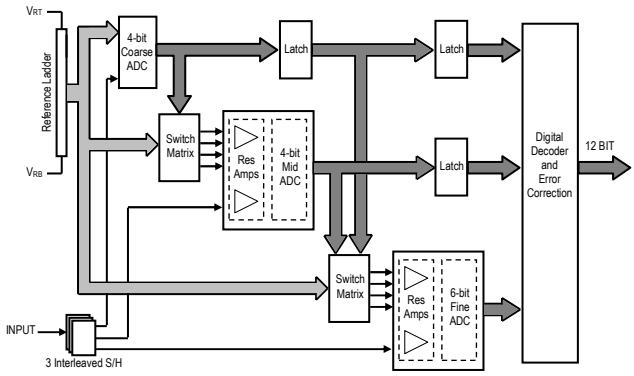

Figure 1. Block diagram of the 12-bit multi-step A/D converter.

To set the inputs of the individual A/D converter stages at the wanted values, a scan-chain is available in the switch-matrix circuit. For mid-range A/D converter measurements, the coarse A/D converter values are prearranged since they determine mid-range A/D converter references. Similarly to evaluate the fine A/D converter both the coarse and mid A/D converter decisions are set to predetermined value. The response of each of the individual A/D converter stages is subsequently routed to the test bus. The sub-D/A converter (implemented as a combination of the reference ladder and the switch matrix) settings are controlled by a serial shift of data through a scan chain that connects all sub-D/A converter registers. To capture the current settings of the sub-D/A converter, it is possible to freeze the contents of the sub-D/A converter registers in normal mode and shift out the data via the scan-chain. A test control bit per sub-D/A converter is available to adjust (increase) the reference current to obtain an optimal fit of sub-D/A converter output range to the A/D converter input range.

B. Process Variation Monitoring Based Calibration

Although a multi-step A/D converter makes use of a considerable amount of digital logic, most of its signal-processing functions are executed in the analog domain. Consequently, the conversion process is susceptible to analog circuit and device impairments. The primary static error sources present in each stage of a multi-step A/D converter are systematic decision stage offset errors λ, stage gain errors η, and errors in the internal reference voltages γ. To facilitate the measurement of these fluctuations, an evaluation strategy as depicted in Figure 2 is proposed. The algorithm inputs are the outputs of each stage of the multi-step A/D converter, and outputs of die-level process monitor (DLPM) circuits and temperature sensors. The desired output is collected at the output of the following stage (back-end) and subtracted from the corresponding nominal value. The algorithm gives the required information to the digital pattern generator, whose outputs steer the calibration D/A converter (implemented as a current-steering DAC), thereby closing the calibration loop. The temperature sensor based on [15] registers any on-chip temperature changes, and, if required, updates the estimation algorithm. The DLPM measurements are directly related to asymmetries between the branches composing the circuit; for all primary error sources, we derive separate DLPMs by extracting (replicating) the targeted error contributor of each stage (e.g. λ, η, and γ). The primary reason for replicating the error contributors is to avoid large added loading of the test scheme on the circuits in sensitive analog signal paths. Additionally, by separating DLPMs from the signal path, the monitors can be designed to maximize the sensitivity of the circuit to the target parameter to be measured. A discrimination window for various die-level process monitors is defined according to the rules of the multi-step A/D converter error model [10].

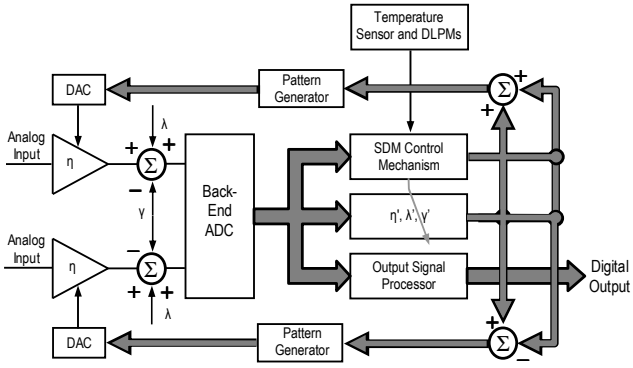

Figure 2. Conceptual view of the calibration loop.

III. DESIGN OF DUAL-RESIDUE MULTI-STEP A/D CONVERTER

A. Time-Interleaved Sample-and-Hold

The sampling rate of a system is further increased by a using time-interleaved technique [16], where a higher sampling rate is obtained by running the system in parallel, although at different clock phases. However, in the front-end S/H, where the clock is used to sample a continuous time signal, any deviation of the sampling moment from its ideal value results in an error voltage in the sampled signal equal to the signal change between these two moments. The clock skew between the sampling clocks of distributed S/H circuits can be calibrated by measuring its value and controlling tunable delays of a DLL [17]. Nevertheless, in general, calibration of the skew between S/H circuits has two significant drawbacks. First, skew measurement is complex and second, the tuning of the delays requires high accuracy from the calibration hardware and algorithm. Alternatively, timing alignment within the

required accuracy can be obtained by using a master clock [18] to synchronize the different sampling instants and by careful design while matching the channels clock and input signals lines [19]. In this design, a similar approach is followed: besides the extensive shielding and matching of the clock lines, the delays of any active buffers within the clock distribution network are kept to the minimum.

Besides timing mismatch, time-interleaved S/H suffers from offset, gain and bandwidth mismatch. One limitation of the offset cancelling method [20] from a systems point of view is the fact that the static offset has to be measured before the calibration. The gain mismatch can be calibrated digitally by measuring the reference levels and storing them in a memory. The ideal output code can be recovered using these measured reference levels [21]. In our implementation the resulting *dc* offset is mainly cancelled with design percussions, such as differential signal path, bottom plate sampling, small feedback switches, opamp high common-mode rejection ratio and by using the closed loop sampling architecture such that consequent offset mismatch is sufficiently low for the required resolution. By dimensioning the open loop *dc*-gain of the operational amplifiers large enough, the effect of gain mismatch is suppressed below the quantization noise level. With careful sizing and layout, capacitor matching sufficient for twelve bit resolution is achieved. By increasing the bandwidth, the impact of the bandwidth mismatch at the signal frequency becomes lower. For this reason, the bandwidth of each sample-and-hold unit has been chosen larger than what is required when just looking at signal attenuation.

B. Stage Design

To maximize the settling time of the sub-D/A converter output, i.e. to achieve a high conversion speed, the coarse and mid A/D converter should be able to provide its output to the sub-D/A converter as soon as possible after the S/H circuit samples the input and enters the hold mode. Therefore, the coarse and mid A/D converter are of parallel, flash type [22] as it provides the highest throughput rate. It should be noted that insufficient settling in coarse and mid A/D converter or mismatch in coarse and mid comparators is directly translated into a quantization error and appears as a shift in the location of the quantization step causing missing codes. To cope with these errors, we have applied over-range and digital correction [23] technique. The low comparator offset is achieved as a result of signal amplification in the preamplifier circuits, the large transresistance of the current-to-voltage conversion, the two-phase clocking scheme [24], which reduces the number of devices that contribute to the offset, and finally with the choice of appropriate transconductance ratios. As a result of the absence of offset compensation, the clock frequency is high.

To reduce power consumption of the 6-bit fine A/D converter, the folding and interpolation technique [25] is applied. In order to increase the intrinsic resolution, more zero-crossings (e.g. necessary for the digital output code transitions) have to be created across the input range. This can be achieved by increasing the number of folding amplifiers at the input or by increasing the interpolation factor. However, these approaches result in increased power consumption, and degraded speed performance. Alternatively, the number of foldings in each folding signal before interpolation can be increased. Conversely, the transconductance curves of the differential pairs starts overlapping; deteriorating the gain of the folding amplifier. In this design, to alleviate the problem of overlapping transconductance curves, folding is conducted at a lower frequency in each stage [26].

The implemented sub-D/A conversion is based on resistor-ladder architecture since it is relatively simple and inherently monotonic as long as the switching elements are designed correctly. Additionally, the DNL of resistor-ladder is relatively low compared to other architectures. Switches in switch matrix are simple CMOS switches designed to have low enough on-resistance to provide sufficient bandwidth for twelve bit settling of the reference signals on the residue amplifiers.

C. Inter-Stage Design

In a multi-step A/D converter, an error in the gain stage causes a non-linearity in the input to output transfer characteristic. If a gain error in the residue amplifier occurs, the total range of the residue signal will be adjusted causing an error in the analog input for the next stage. As a consequence the residue signal will not fit in the subsequent A/D converter range. In our design, the implemented dual-residue signal processing [27] spreads the errors of the residue amplifiers over the whole mid and fine range, which results in an improved linearity. According to quantization decision of the previous stage, a first and a second residue amplifier pass the difference between the analog signal and the closest and the second closest quantization level, respectively. By passing both residues to subsequent stages, information is propagated about the exact size of the quantization step, as the sum of the two residues is equal to the difference between the two quantization levels. The absolute gain of the two residue amplifiers is therefore not important, providing that both residue amplifiers match and have sufficient signal amplitude to overcome finite comparator resolution.

D. Multi-Stage Circuit Calibration (MSCC) Algorithm

Based on the predefined inputs and current error estimates, proposed calibration algorithm based on the steepest-descent method (SDM) [28] (Figure 2) involves the creation of an estimation error *e*, by comparing the estimated output $D'_{out}(t)$ to a desired response $D_{out}(t)$. Statistical data extracted through the DLPM measurements provide the SDM estimates $(W')^T=[\eta',\gamma',\lambda']$ with an initial value. The automatic adjustment of the input weights $(W')^T$ is performed in accordance with the estimation error *e*. At each iteration, the algorithm requires knowledge of the most recent values, $D_{in}(t)$, $D_{out}(t)$ and $W'(t)$. During the course of adaptation, the algorithm recurs numerous times to effectively average the estimate and to find the best estimate of weight *W*. The temporary residue voltage in input D_{in} needs to be updated after each iteration time to improve the accuracy, which can be done by using the current error estimate *W'*. As temperature can vary significantly from one die area to another, these fluctuations in the die temperature influence the device characteristics. In the implemented system, the temperature sensors register any on-chip temperature changes, and the estimation algorithm update the *W'* with a forgetting factor, ζ [29].

Algorithm

Initialization
- Initialize the input vector $D_{in}(0)$
- Force the inputs and collect the desired output $D_{out}(0)$
- Measure and set the initial value of the weights $W'(0)$
- Initialize the steepest descent update step μ=1
- Initialize the forgetting factor ζ

Data collection
- Collect N samples from the DLPM and temperature sensors
- Collect N samples from the AD converter

Update parameter estimate
1. Update the input vector $D_{in}(t+1)$ based on current available $W(t)$
2. Calculate the error estimate $W'(t)$
3. Generate the output estimate $D'_{out}(t)= D_{in}(t)\times W'(t)$
4. Calculate the estimation error $e(t) = D'_{out}(t)-D_{out}(t)$
5. Calculate the error estimate $W'(t+1)= W'(t)-\mu\times D_{in}(t)\times e(t)$
6. If $W'(t+1)> W'(t)$ decrease step size μ and repeat step 5
7. Increase the iteration index, t and repeat steps 1-6 for best estimate
8. Denote the final value of W' by W_l'
9. If temperature changes update $W'(t+1)=\zeta W'(t)+(1-\zeta) W_l'(t+1)$

IV. Experimental Results

A prototype 12 bits multi-step A/D converter with dedicated embedded process monitors was fabricated in a standard single poly, six metal 90 nm CMOS (Figure 3). The stand-alone A/D converter occupies an area of 0.75 mm^2 operates at 1.2 V supply voltage and dissipates 55 mW (without output buffers). Dedicated embedded monitors (12 per stage subdivided into three specific groups and placed in and around the partitioned multi-step A/D converter) and the complete DfT are restricted to less than 10% of the overall area and consume 8 mW and 0.4 mW when in active and passive mode, respectively. Each DLPM consists of 12 differential pairs or ladder resistors corresponding to gain-, decision- or referenced-based monitor, respectively. The DLPM circuits are small and stand-alone, they match the physical layout of the extracted device under test, and consume no power while in off state. Additionally, the test-chip contains a temperature sensor (located between coarse A/D converter and fine residue amplifiers), which consumes only 11 µW. The MSCC algorithm requires about 1.5k logic gates as calibration overhead, occupies an area of 0.14 mm^2 and consumes 11 mW of power.

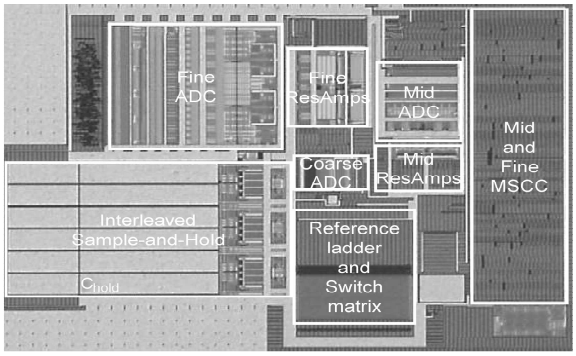

Figure 3. Chip micrograph.

The test shell contains all functional control logic, the digital test bus, a test control block (TCB) and a CTAG isolation chain. Testing of each stage is performed sequentially starting from the first stage. Since there is no feedback from the mid and fine A/D converters to the coarse result value, it is not necessary to set these two A/D converters at a fixed value to test the coarse A/D converter. However, since the calibration D/A converter settings do show in the mid A/D converter results, the sub-D/A converter is set to a known value to prevent interference with the mid A/D converter test results. Similar to the mid A/D converter, the fine A/D converter cannot be monitored directly due to the overlap in the A/D converter ranges. The predefined input signals are extracted when the A/D converter operates in a normal application mode. At a certain moment the scan chains are set to a hold mode to acquire the requested value. Now, the residue signals derived through the predefined input signals evaluate the fine A/D converter performance. The calibration signals need to be active as well for the fine A/D converter test. To verify offsets, a similar procedure as in the mid A/D converter is followed. The calibration D/A converter settings have to be known and set to a known value to prevent interference with test results.

The calibration technique was verified for all stages with full scale inputs. If the analog input to the calibrated A/D converter is such that the code transition is i, then the code transition of the ideal A/D converter is either i or $i+1$. The offset between the digital outputs of these two converters for the range of analog inputs is denoted Δ_{i1} and Δ_{i2}, respectively. If a calibrated A/D converter has no errors in the internal reference voltages γ and neither has stage gain errors η, the difference between the calibrated and ideal A/D converter outputs is constant regardless of the analog input, thus $\Delta_{i1}=\Delta_{i2}$. If errors γ and η are included, then the calibrated A/D converter shows unique missing codes. The difference between Δ_{i1} and Δ_{i2} gives the error due to missing codes that occur when the ideal A/D converter changes from code i to code $i+1$. The unique error due to missing codes at all other transitions can be measured in a similar manner. With errors from missing codes at each measured transition, the calibrated A/D converter stage is corrected by shifting the converter's digital output as a function of the transition points such that the overall transfer function of the calibrated A/D converter is free from missing codes. As long as the input is sufficiently rapid to generate a sufficient number of estimates of Δ_{i1}, Δ_{i2}, for all i, there is no constraint on the shape of the input signal to the A/D converter. A constant offset between the calibrated and ideal A/D converter appears as a common-mode shift in both Δ_{i1} and Δ_{i2}. Since the number of missing codes at each code transition is measured by subtracting Δ_{i2} from Δ_{i1}, the common mode is eliminated and thus input-referred offsets of the calibrated A/D converter have no impact in the calibration scheme (under the practical assumption that the offsets are not large enough to saturate the output of the converter stages). The mean-square error for million samples is 10^{-1}. The largest correction values significantly decrease with the amount of samples. As an ideal A/D converter offers an ideal reference for the calibrated A/D converter, the error signal used for the algorithm adaptation is highly correlated with the error between them, thus steady state convergence occurs within a relatively short time interval. Different λ, η, and γ are generated randomly, so that the relative errors are uniformly distributed in the interval [-0.1,0.1]. At first, μ is set to 1/4 to speed up the algorithm, then μ is set to 1/64 after 1000 iterations to improve the accuracy.

	[2]	[3]	[4]	[5]	[6]	[7]	**[This work]**
CMOS Technology	*0.6 µm*	*0.35 µm*	*0.18 µm*	*0.13 µm*	*90 nm*	*90 nm*	*90 nm*
Resolution (bit)	*12*	*12*	*12*	*12*	*12 (nom)*	*12*	*12*
Supply voltage (V)	*5*	*3.3*	*1.8*	*1.2*	*1.2*	*1.2*	*1.2*
Sample rate (MS/s)	*33*	*20*	*50*	*120*	*100*	*200*	*60*
Eff. bandwidth (MHz)	*16*	*10*	*25*	*60*	*50*	*91*	*30*
DNL (LSB)	*±0.8*	*±0.42*	*±0.26*	*±0.3*	*±0.54*	*+0.8/-0.6*	*± 0.7*
INL (LSB)	*±1*	*±0.75*	*±0.72*	*+0.95*	*±368*	*+1.3/-1.7*	*±1.2*
SNDR (dB)	*70.3*	*70.2*	*64*	*74.7*	*68.8*	*61.6*	*68.6*
Calibration	*Piecewise Lin.*	*Nested*	*DCL*	*off chip*	*HDC*	*LMS*	*SDM*
Power (mW)	*650*	*231*	*18.4*	*51.6*	*130*	*348*	*55*
Area (mm^2)	*3*	*7.5*	*0.26*	*0.56*	*4*	*1.36*	*0.75*

TABLE I– SUMMARY OF A/D CONVERTER PERFORMANCE AND COMPARISION WITH PRIOR ART

	before	*(0 ºC)*	*(30ºC)*	*(90ºC)*
Coarse A/D Converter				
DNL	*±0.5 LSB*	*±0.5 LSB*	*±0.4 LSB*	*±0.4 LSB*
INL	*±0.7 LSB*	*±0.7 LSB*	*±0.6 LSB*	*±0.6 LSB*
THD	*-26.1 dB*	*-26.4 dB*	*-26.7 dB*	*-26.5 dB*
SNR	*23.7 dB*	*23.9 dB*	*24.3 dB*	*23.8 dB*
Mid A/D Converter				
DNL	*±0.7 LSB*	*±0.7 LSB*	*±0.5 LSB*	*±0.6 LSB*
INL	*±1.8 LSB*	*±0.8 LSB*	*±0.6 LSB*	*±0.7 LSB*
THD	*-13.8 dB*	*-24.8 dB*	*-26.1 dB*	*-25.3 dB*
SNR	*12.4 dB*	*21.3 dB*	*23.5 dB*	*22.4 dB*
Fine A/D Converter				
DNL	*±0.9 LSB*	*±0.9 LSB*	*±0.6 LSB*	*±0.8 LSB*
INL	*±2.6 LSB*	*±1.0 LSB*	*±0.9 LSB*	*±0.9 LSB*
THD	*-18.3 dB*	*- 33.7 dB*	*-35.8 dB*	*-33.2 dB*
SNR	*15.6 dB*	*29.5 dB*	*31.4 dB*	*29.1 dB*
Total A/D Converter				
DNL	*±1.4 LSB*	*±1.2 LSB*	*±0.7 LSB*	*±1.1 LSB*
INL	*±4.1 LSB*	*±1.5 LSB*	*±1.2 LSB*	*±1.4 LSB*
THD	*-46.6 dB*	*-69.4 dB*	*-73.5 dB*	*-70.9 dB*
SNR	*41.5 dB*	*67.3 dB*	*70.3 dB*	*68.7 dB*

TABLE II– SUMMARY OF THE CALIBRATION PERFORMANCE

A summary of the converter performance at 30°C and comparison with previous works is shown in Table I. Calibration results measured at several temperatures are summarized in Table II. A code density test was conducted to obtain static linearity of the proposed A/D converter. DNL (Figure 4) and INL (Figure 5) are measured with a signal frequency of 1 kHz and 15 MS/s, and THD and SNR are obtained with 25 MHz input signal and 60 MS/s sampling frequency (Figure 6). The largest spike, other than the fundamental input signal, is the spurious harmonic which appears at $fs/3 \pm f_{in}$ and is about 78.1 dB below the fundamental signal. A locked histogram test revealed a 1.6-ps rms jitter in the system including the clock generator, the synthesizer, the A/D comparator chip and the board, which translates to a 70.4 dB SNR at 30 MHz input frequency. This confirms the observation that the performance of this converter is limited by the clock jitter at high input frequencies. The measured behavior of the temperature monitor shows the typical bandgap-curve which reaches a maximum at 810 mV close to the target of 800 mV without trimming. Results from 35 prototype samples show a standard deviation of the bandgap output voltage of 4.5mV. The temperature sensor switches at intervals of 10ºC as measured on a digital production IC tester. Mismatch simulations indicate that an absolute untrimmed accuracy of the switching points is in the order of 5ºC. This accuracy is limited by the matching performance of the MOS amplifier which in turn is restricted by the sizes of the transistors in the library style layout. We observe that the improvement of DNL and INL is coincident with the fact that the mismatch increases when decreasing the temperature. Therefore, as the worst case mismatch and temperature condition, the lower end (0°C) of the used temperature scale (0°C to 90°C) is observed. The linearity measurements show bathtub-like features since at the higher temperature end, mobility degradation deteriorates the circuit performance. The DLPM measurements show that at optimal temperature (30°C), the standard deviation $Stdev(\Delta V_{Tsat})$ decreases by 0.16mV. This compares reasonably well with the measured improvement in I_{Dsat} matching of 0.032%. The threshold voltage matching coefficient A_{VT}, the standard deviation of percent ΔI_D and the current matching coefficient A_{ID} improve by 0.3mVµm, 0.032% (0.036µA), and 0.06%µm, respectively.

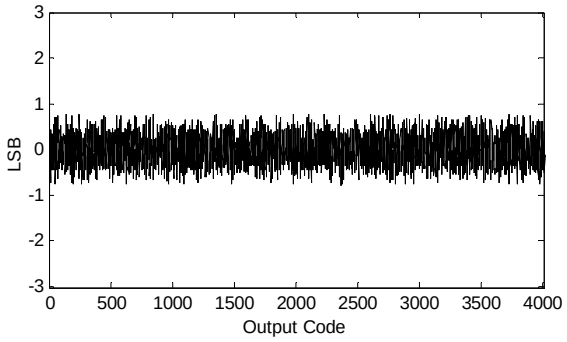

Figure 4. Measured DNL after calibration.

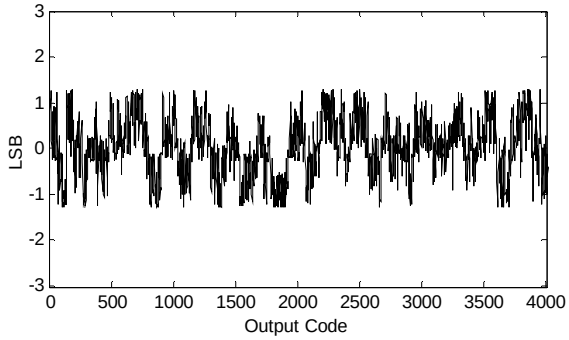

Figure 5. Measured INL after calibration.

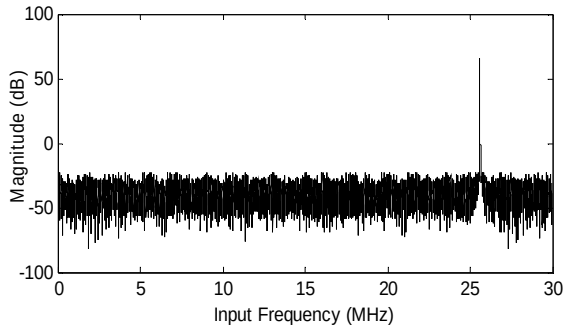

Figure 6. Measured frequency spectrum at 60 MS/s with an input frequency of 25.6 MHz

V. CONCLUSION

The feasibility of the calibration method has been verified by experimental measurements from the silicon prototype fabricated in standard single poly, six metal 90 nm CMOS. The stand-alone A/D converter occupies an area of 0.75 mm^2 operates at 1.2 V supply voltage and dissipates 55 mW (without output buffers). The calibration algorithm requires about 1.5k logic gates, occupies an area of 0.14 mm^2 and consumes 11 mW of power. Fast identification of excessive process parameter variation effects is facilitated at the cost of at most 10% area overhead, and 8 mW and 0.4 mW of power consumption when in active and passive mode, respectively.

ACKNOWLE DGMENT

The authors acknowledge the contributions of M. Barragan, S. Krishnan, P. Pavithran and V. Zieren.

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